Operation and Design of Multilevel Inverters

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3 / Operation and Design of Multilevel Inverters

The concept of utilizing multiple small voltage levels to perform power conversion was patented by an MIT researcher over twenty years ago [1,2]. Advantages of this multilevel approach include good power quality, good electromagnetic compatibility (EMC), low switching losses, and high voltage capability. The main disadvantages of this technique are that a larger number of switching semiconductors are required for lower-voltage systems and the small voltage steps must be supplied on the dc side either by a capacitor bank or isolated voltage sources. The first topology introduced was the series H-bridge design [1]. This was followed by the diode-clamped [2-4] converter which utilized a bank of series capacitors. A later invention [5] detailed the flying capacitor design in which the capacitors were floating rather than series-connected. Another multilevel design involves parallel connection of inverter phases through inter-phase reactors [6]. In this design, the semiconductors block the entire dc voltage, but share the load current. Several combinational designs have also emerged [7] some involving cascading the fundamental topologies [8-12]. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels.

Recent advances in power electronics have made the multilevel concept practical [1-19]. In fact, the concept is so advantageous that several major drives manufacturers have obtained recent patents on multilevel power converters and associated switching techniques [20-26]. Furthermore, several IEEE conferences now hold entire sessions on multilevel power conversion. It is evident that the multilevel concept will be a prominent choice for power electronic systems in future years, especially for medium-voltage operation.

This chapter describes the fundamentals of multilevel power conversion. Some background material is provided followed by the mathematical details of the power and control sections.

3.1 MULTILEVEL CONCEPTS AND NOTATION

This section introduces the general multilevel power converter as well as the advantages of using an increasing number of voltage levels. Common mathematical notation is also introduced for use in subsequent sections.

3.1.1 Multilevel power conversion system

Figure 3.1-1 shows a motor drive which will be used to exemplify general multilevel concepts. Although an inverter is used as the basis for this discussion, the multilevel converter can be used in active rectifier [13,14] and flexible AC transmission

systems (FACTS) applications [15,16]. From a system point of view, the multilevel inverter has been inserted in place of a standard inverter. Herein, n is used to represent the number of voltage levels and can be set to two in order to represent a standard inverter. An output L-C-R filter has been placed in-between the inverter and motor load in order to meet harmonic requirements at the motor terminals.

3.1.2 Voltage level notation

Herein, switching states s_a, s_b, and s_c will be defined for the *a*- *b*- and *c*-phase respectively. Each switching state has a range from 0 to $(n-1)$ in order to represent the complete number of switching levels. Assuming proper operation, the inverter output line-to-ground voltages (defined from the phase nodes *a*, *b*, and *c* to the negative rail of the dc bus) follow the switching states as

$$\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} = \left(\frac{v_{dc}}{n-1} \right) \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} \tag{3.1-1}$$

From Figure 3.1-1, it can be seen that the modulator determines the switching states; thereby depicting the inverter output voltages. This system is somewhat idealized since, in practice, the output of the modulator is the transistor signals. Furthermore, the line-to-ground voltages may vary a bit from (3.1-1)-(3.1-3) since the voltage levels are typically made up from a series capacitor bank. However, these issues will be more formally addressed in the following section relating to the specific multi-level hardware. Figure 3.1-2 shows inverter line-to-ground voltages for several values of n. According to the modulation process (described in detail in a later section), the output is an ideal sine-wave with switching harmonics. It is fairly obvious that increasing the inverter levels results in an inverter output voltage that more closely tracks the ideal sinusoidal output. As a final note, various voltage definitions will be described for clarity. The line-to-neutral voltages may be determined directly from the line-to-ground voltages by [27]

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \tag{3.1-2}$$

Inverter line-to-line voltages are related to the line-to-ground voltages by

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \tag{3.1-3}$$

Figure 3.1-3 shows the switching state, line-to-ground voltage, line-to-neutral voltage, and line-to-line voltage for the case where $n = 9$. Therein, the line-to-ground voltage contains a third harmonic component which is added in order to maximize the inverter output voltage [27]. Therein, it can be seen that the line-to-neutral and line-to-line voltages do not contain the third harmonic. Also, it is interesting to note that these voltages contain more levels than the original line-to-ground voltages. It is easily understood that there are $2n-1$ line-to-line voltage levels consisting of *n* positive levels, *n* negative levels, and zero. In Figure 3.1-3, these seventeen voltage levels can be clearly seen in v_{ab}. As it turns out, there are $4n-3$ line-to-neutral voltage levels which works out to thirty-three for the nine-level inverter. However, the switching between the levels is not perfectly even since all three phases are involved.

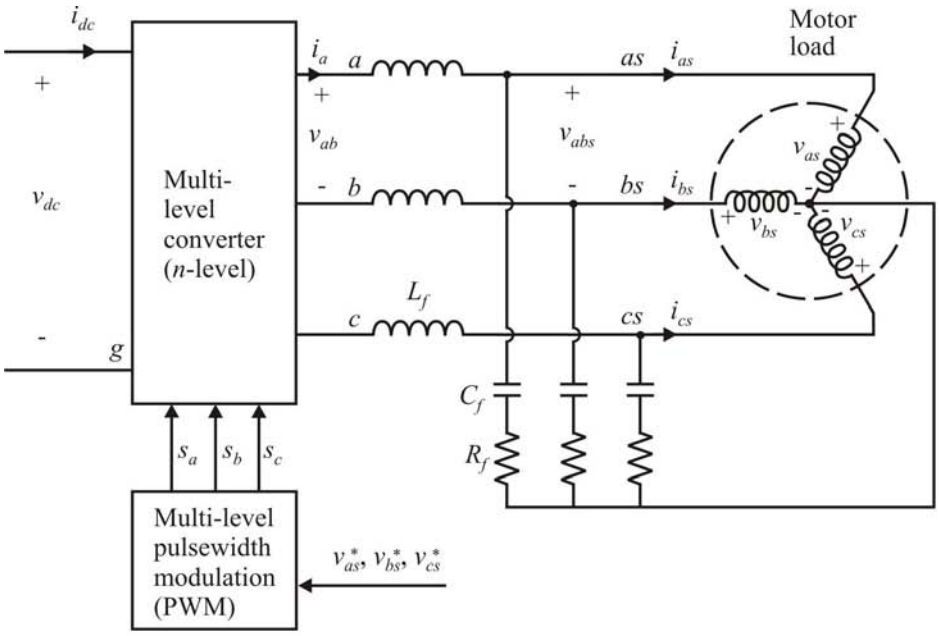

Figure 3.1-1. Multi-level converter system.

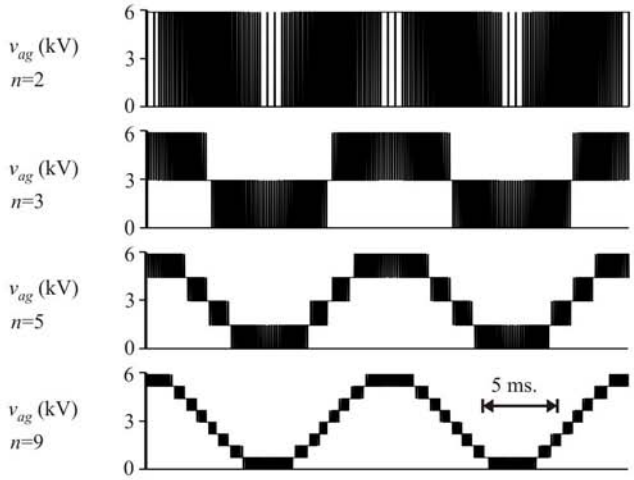

Figure 3.1-2. Output voltage for various level numbers.

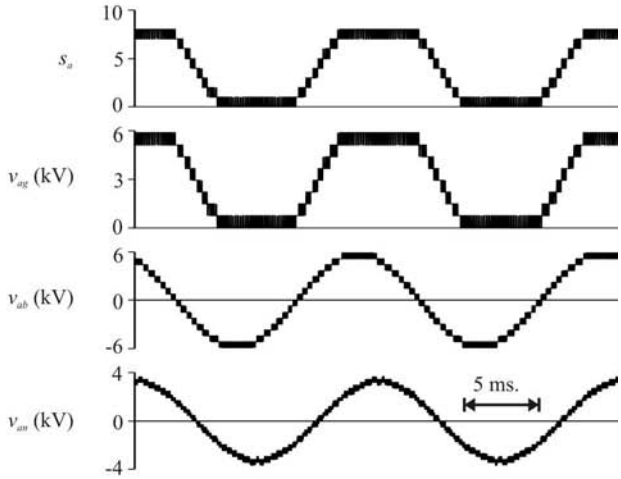

Figure 3.1-3. Nine-level inverter voltage waveforms.

3.1.3 Voltage vectors

One good method of gaining insight into the operation of multilevel inverters is to view the voltages in the *q-d* stationary reference frame. The resulting vector plot contains information from all three phases and displays redundant switching states. The plot is particularly useful for comprehending the higher number of switching states as compared to the two-level inverter. In addition, some mathematical relationships and derivations can be readily obtained from the vector plot. The vector diagram has also been used to formulate multilevel modulation. However, it will be shown later that this is more readily accomplished in the time domain.

The inverter voltages can be expressed in the arbitrary *q-d* reference frame by [27]

$$\begin{bmatrix} v_{qn} \\ v_{dn} \\ v_{0n} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos\left(\theta-\frac{2\pi}{3}\right) & \cos\left(\theta+\frac{2\pi}{3}\right) \\ \sin(\theta) & \sin\left(\theta-\frac{2\pi}{3}\right) & \sin\left(\theta+\frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{3.1-4}$$

Considering (3.1-1), (3.1-2), and that the angle is $\theta = 0$ for the stationary reference frame, the *q-d* stationary voltages can be expressed in terms of the switching states by

$$v_{qn}^{s} = \frac{v_{dc}}{3(n-1)}(2s_a - s_b - s_c) \tag{3.1-5}$$

$$v_{dn}^{s} = \frac{v_{dc}}{\sqrt{3}(n-1)}(s_c - s_b) \tag{3.1-6}$$

The vector plot is created by graphing the voltage vector defined by

$$v_{sw} = v_{qn}^{s} - j\,v_{dn}^{s} \tag{3.1-7}$$

for all possible switching states. Figure 3.1-4 shows the vector plot for the three-level inverter. Therein, each vector v_{sw} is denoted with a unique number. For the general *n*-level inverter vector number can be related to the switching state by

$$sw = n^2 s_a + n\,s_b + s_c \tag{3.1-8}$$

Figure 3.1-4 shows that there are several vectors which result from a number of switching states. This switching state redundancy occurs since the common-mode component of the switching states is not included in the two-dimensional voltage vector plot. For the general *n*-level three-phase inverter, there are

$$n_{sw} = n^3 \tag{3.1-9}$$

switching states and

$$n_{vec} = 3n(n-1)+1 \tag{3.1-10}$$

voltage vectors.

Figure 3.1-5 shows the voltage vector plots for two- three- five- and nine-level inverters. In this domain, it is clear that the higher level inverters can provide less voltage deviation resulting in better harmonic performance.

3.1.4 Redundant switching states

The redundant switching states seen in Figure 3.1-4, provide some flexibility in the multilevel systems and will be used to achieve control objectives in later sections. For now, it is helpful to define some basic redundant state relationships. The number of redundant states for a particular switching state set can be calculated by

$$n_{RSS} = n - (s_{max} - s_{min}) \tag{3.1-11}$$

where s_{max} and s_{min} are the maximum and minimum of the switching state set or

$$s_{max} = \max(s_a, s_b, s_c) \tag{3.1-12}$$

$$s_{min} = \min(s_a, s_b, s_c) \tag{3.1-13}$$

Since this redundancy involves all three phases, it is referred to as joint-phase redundancy. It will be shown in later sections that some multilevel topologies have redundancy within each phase. This per-phase redundancy can be used or combined with joint-phase redundancy to achieve certain control objectives such as capacitor voltage balancing.

3.1.5 Multilevel inverter performance

This section looks at multilevel inverter system performance for various numbers of voltage levels. To perform this comparison, a 1 MVA, 800 kW, 4.16 kV 60 Hz motor drive system is used. The inverter structure is that of Figure 3.1-1 with a dc voltage of 6 kV. The inverter modulation is operating at 5 kHz with a modulation index that is 98% of the maximum. Figure 3.1-6 shows the inverter waveforms with

a two-level inverter. The line-to-neutral voltage v_{an} and line-to-line voltage v_{ab} result from the line-to-ground voltage as described above yielding three levels in v_{ab} and five levels in v_{an}. The filter is sized so that the load voltage has a total harmonic distortion (THD) of 2.5%. As a result, the phase voltage v_{as} contains little harmonic content and the current waveform is nearly sinusoidal. Figure 3.1-7 shows the performance for a nine-level inverter under the same operating conditions. Due to the higher number of voltage levels, a smaller output filter can be used to obtain the same voltage THD at the load terminals.

The above studies were performed with three- and five-level inverters for further comparison. The results are shown in Figure 3.1-8. Therein, the line-to-neutral voltage THD, output filter size, and inverter power losses are shown versus number of voltage levels. Considering the THD, it can be seen that there is a significant difference between the two- and three-level inverters. However, as the number of levels becomes large, the change in THD is not as great. As expected, the output filter size has a similar characteristic versus levels as the THD. In this case, a 50 μF capacitor was used for all studies and the inductor was sized to set the phase voltage THD. The resistor was used to limit the gain at the resonant frequency. Although more advanced filter techniques can be used the resistor could be sized in these examples so that the power losses were less than 2% and the effect on filter performance was negligible. The conduction losses are fairly constant, but the switching losses decrease by a factor of three from the two-level to the nine-level case. One might expect that the switching losses would decrease by a factor of $n-1$ or eight. In this example, a flying capacitor inverter [5] was used for the implementation of the various levels and some of the savings in switching losses were sacrificed in order to balance the flying capacitors. In this way, the inverter can be operated from a single dc source as shown in Figure 3.1-1.

It should be pointed out that the decrease in filter inductance size is offset by the need for flying capacitors. In the case of the nine-level inverter, seven 1000 μF capacitors were needed having an average voltage of 3000 V and an average rms current of 50 A. The exact sizing of these capacitors depends on the tolerable voltage ripple. In this example, the voltage ripple for each capacitor was around 5%. Although these tradeoffs exist, the multilevel inverter has some distinct advantages. Besides lower switching losses, the output voltage dv/dt is lowered which improves EMC and also reduces stresses on the filter circuitry. Additionally, the multilevel inverter avoids series connection of devices for higher-voltage systems. In the above examples, 1200 V, 300 A IGBTs were used for the switching devices. The two-level inverter had eight IGBTs in series to make up each switch. As a practical matter, switching the series IGBTs so that they dynamically share the bus voltage is a major challenge. Although it may be possible to use fewer higher-voltage IGBTs instead, the switching characteristics of those IGBTs would make a 5 kHz switching frequency unreasonable. However, lowering the switching frequency would lead to a larger filter size. The nine-level inverter also used eight IGBTs, but they are not

directly connected in series and the flying capacitors fix their voltage to one-eighth of the dc voltage.

The above example qualitatively shows the advantages of multilevel power conversion. Several details about the topology and control were omitted for brevity, but the following sections cover the specifics. In addition, cascaded topologies will be presented. The advantage of these systems is that they can effectively operate with a higher number of levels for a given number of semiconductor devices. In particular, the nine-level inverter example above can be replaced with a cascaded inverter which has half as many transistors.

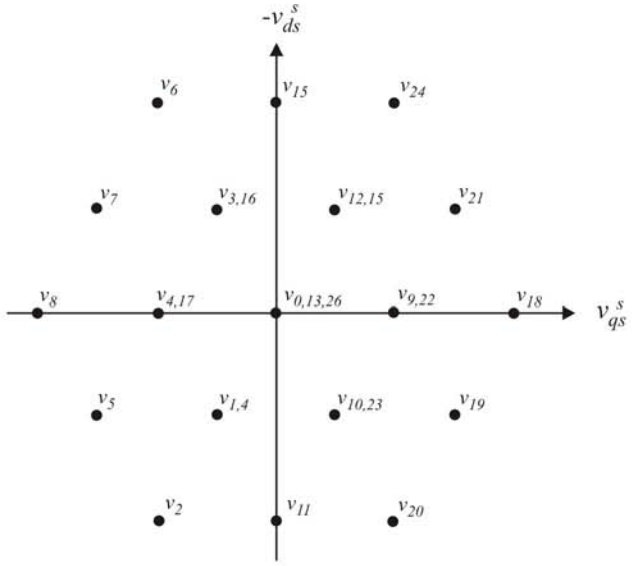

Figure 3.1-4. Voltage vector plot for the three-level inverter.

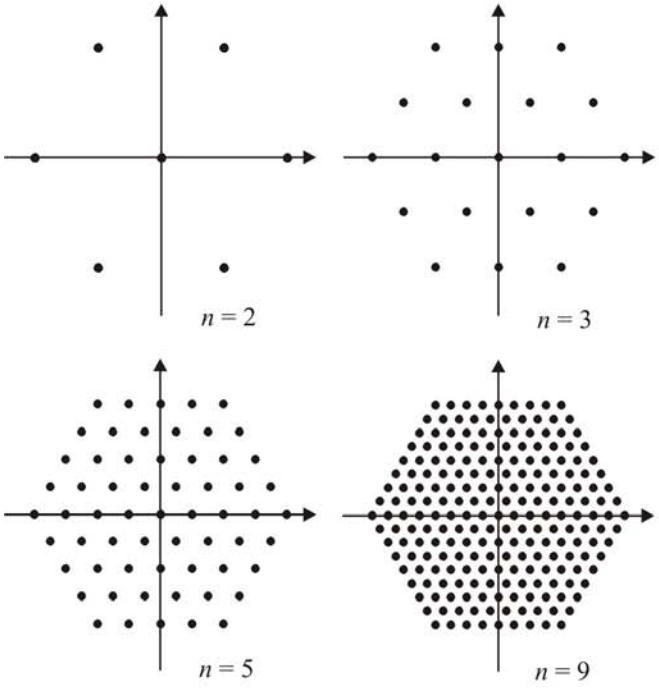

Figure 3.1-5. Voltage vector plots.

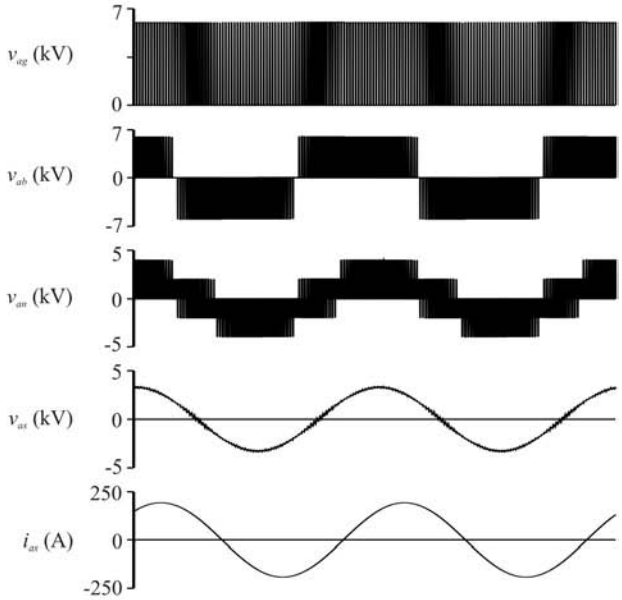

Figure 3.1-6. Nine-level inverter waveforms.

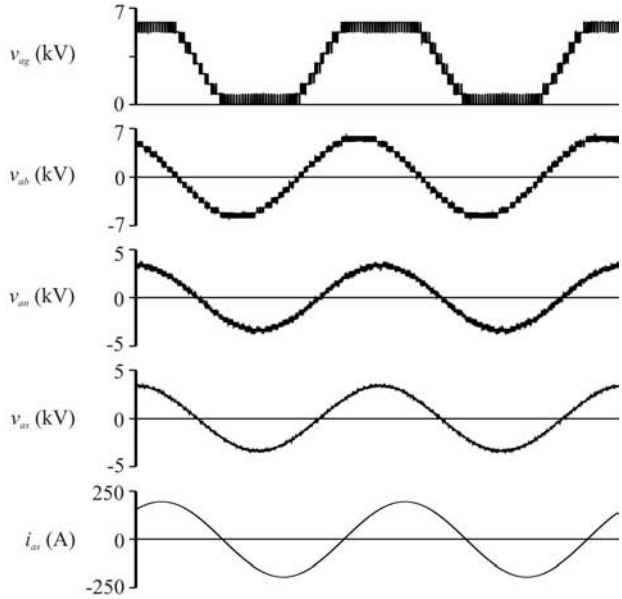

Figure 3.1-7. Nine-level inverter waveforms.

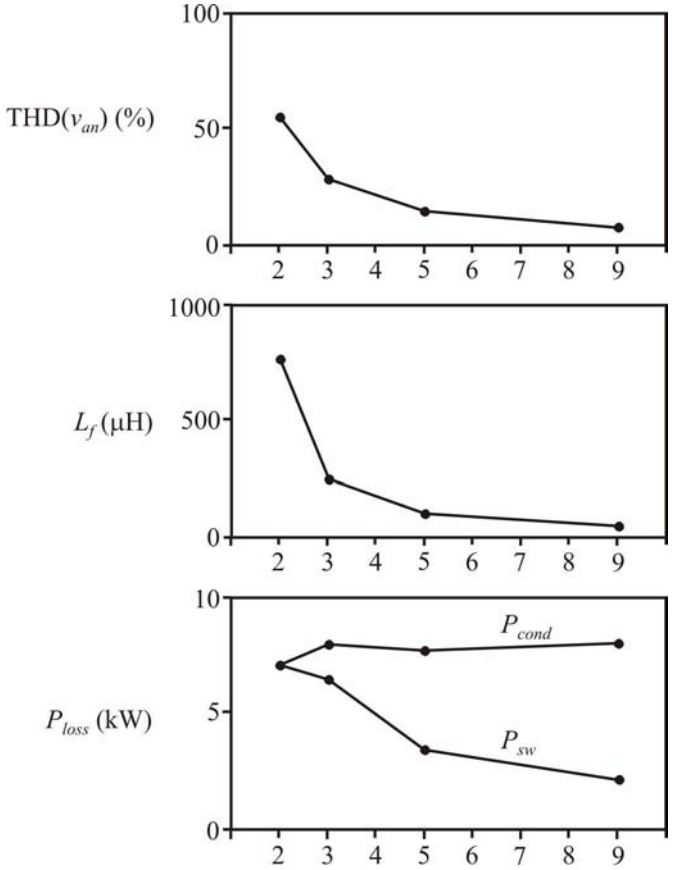

Figure 3.1-8. THD, filter inductance, and losses versus number of voltage levels.

3.2 MULTILEVEL INVERTER POWER SECTION

3.2.1 Diode-clamped multilevel inverter

The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series bank of capacitors. According to the original invention [2], the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels [3] where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was introduced [3]. However, with an even number of voltage levels, the neutral point is not accessible, and the term multiple point clamped (MPC) is sometimes applied [4]. Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been mostly limited to the three-level. Because of industrial developments over the past several years, the three-level inverter is now used extensively in industry applications [20-26]. Although most applications are medium-voltage, a three-level inverter for 480V is on the market [20].

Figure 3.2-1 shows the topology of the three-level diode-clamped inverter. Although the structure is more complicated than the two-level inverter, the operation is straightforward and well known [4]. In summary, each phase node (*a*, *b*, or *c*) can be connected to any node in the capacitor bank (d_0, d_1, or d_2). Connection of the *a*-phase to junctions d_0 and d_2 can be accomplished by switching transistors T_{a1} and T_{a2} both off or both on respectively. These states are the same as the two-level inverter yielding a line-to-ground voltage of zero or the dc voltage. Connection to the junction d_1 is accomplished by gating T_{a1} off and T_{a2} on. In this representation, the labels T_{a1} and T_{a2} are used to identify the transistors as well as the transistor logic (1=on and 0=off). Since the transistors are always switched in pairs, the complement transistors are labeled $\overline{T}_{a1}$ and $\overline{T}_{a2}$ accordingly. In a practical implementation, some dead time is inserted between the transistor signals and their complements meaning that both transistors in a complementary pair may be switched off for a small amount of time during a transition [27]. However, for the discussion herein, the dead time will be ignored. From Figure 3.2-1, it can be seen that, with this switching state, the *a*-phase current i_{as} will flow into the junction through diode D_{a1} if it is negative or out of the junction through diode D_{a2} if the current is positive. According to this description, the inverter relationships for the *a*-phase are presented in Table 3.2-1.

Table 3.2-1. Three-level inverter relationships.

s_a	T_{a2}	T_{a1}	v_{ag}	i_{adc1}	i_{adc2}
0	0	0	0	0	0
1	0	1	v_{c1}	i_{as}	0
2	1	1	$v_{c1} + v_{c2}$	0	i_{as}

If each capacitor is charged to one-half of the dc voltage, then the line-to-ground voltage can be calculated by the ideal equation (3.1-1). The dc currents i_{adc1} and i_{adc2} are the *a*-phase components to the junction currents i_{dc1} and i_{dc2} in Figure 3.2-1 respectively.

Extending the diode-clamped concept to four levels results in the topology shown in Figure 3.2-2. A pair of diodes is added in each phase for each of the two junctions. The operation is similar to the three-level inverter with the relationships described in Table 3.2-2.

Table 3.2-2. Four-level inverter relationships.

s_a	T_{a3}	T_{a2}	T_{a1}	v_{ag}	i_{adc1}	i_{adc2}	i_{adc3}
0	0	0	0	0	0	0	0
1	0	0	1	v_{c1}	i_{as}	0	0
2	0	1	1	$v_{c1} + v_{c2}$	0	i_{as}	0
3	1	1	1	$v_{c1} + v_{c2} + v_{c3}$	0	0	i_{as}

The general *n*-level modulator, described in the next section, determines the switching state for each phase. For practical implementation, the switching state needs to be converted into transistor signals. Considering Tables 3.2-1 and 3.2-2, this can be accomplished in general by

$$T_{ai} = \begin{cases} 1 & s_a \geq i \\ 0 & \text{elesewise} \end{cases} \tag{3.2-1}$$

An inverse relationship may also be useful and is given by

$$s_a = \sum_{i=1}^{n-1} T_{ai} \tag{3.2-2}$$

Once the transistor signals are established, general expressions for the *a*-phase line-to-ground voltage and the *a*-phase component of the dc currents can be written as

$$v_{ag} = \sum_{i=1}^{n-1} T_{ai}\, v_{ci} \tag{3.2-3}$$

$$i_{adci} = \left| T_{a(i+1)} - T_{ai} \right| i_{as} \quad \text{for } i = 1, 2, \ldots (n-2) \tag{3.2-4}$$

In (3.2-4), the value of the non-existent transistor is $T_{an} = 0$.

The above relationships may be programmed into simulation software to form a block that simulates one phase of a diode-clamped inverter. A number of blocks can be connected together for a multi-phase system. These equations allow system simulation including capacitor voltage variation. For more simulation detail, the transistor and diode KVL and KCL equations may be implemented. This allows inclusion of the device voltage drops (as well as conduction losses) and the individual device voltages and currents. To express this relationship, consider the general *n*-level *a*-phase diode-clamped structure shown in Figure 3.2-3. Therein, only the upper half of the inverter is considered since the lower half contains complementary transistors and may be analyzed in a similar way. Through the clamping action of the diodes, the blocking voltage of each transistor is the corresponding capacitor voltage in the series bank. Neglecting the clamping diode voltages, an approximate expression for the transistor is

$$v_{Tai} = (1 - T_{ai}) v_{ci} + T_{ai} \left[I_a\, v_{sw} - (1 - I_a) v_d \right] \tag{3.2-5}$$

where v_{sw} and v_d are the transistor and diode on-state voltage drops respectively and I_a is a logic flag representing the direction of the *a*-phase current

$$I_a = \begin{cases} 1 & i_{as} > 0 \\ 0 & \text{elsewise} \end{cases} \tag{3.2-6}$$

By KVL, the clamping diode voltages can be expressed as

$$v_{Di} = \sum_{j=i}^{n-1} \left(v_{cj} + v_{Taj} \right) \tag{3.2-7}$$

By calculation of the diode voltages, it can be seen that the inner diodes block a higher voltage. For example, in the four-level topology the inner diodes must block two-thirds of the dc voltage while the outer diodes block one-third. This is a well-known disadvantage of the diode-clamped topology. For this reason, some authors represent the higher voltage diodes with lower voltage diodes in series [17] or alter the structure of the topology so that each diode blocks the same voltage [18]. The

line-to-ground voltage may be calculated as the dc voltage minus all transistor voltages which leads to

$$v_{ag} = \sum_{i=1}^{n-1} T_{ai} \left[v_{Tai} - I_a v_{sw} + (1 - I_a) v_d \right] \tag{3.2-8}$$

The transistor currents may be expressed by

$$i_{Tai} = T_{ai} \, I_a \, i_{as} \tag{3.2-9}$$

When all transistor signals are on, the negative current does not have a clamping diode path and the freewheeling diode currents may be calculated by

$$i_{DTai} = i_{as} (1 - I_a) \prod_{j=1}^{n-1} T_{aj} \tag{3.2-10}$$

The clamping diode currents may be calculated by KCL resulting in

$$i_{Dai} = i_{Ta(i-1)} - i_{Tai} \tag{3.2-11}$$

Finally, the capacitor junction currents may be expressed as the difference of two clamping diode currents. The expression reduces to

$$i_{dci} = \left| T_{ai} - T_{a(i-1)} \right| i_{as} \tag{3.2-12}$$

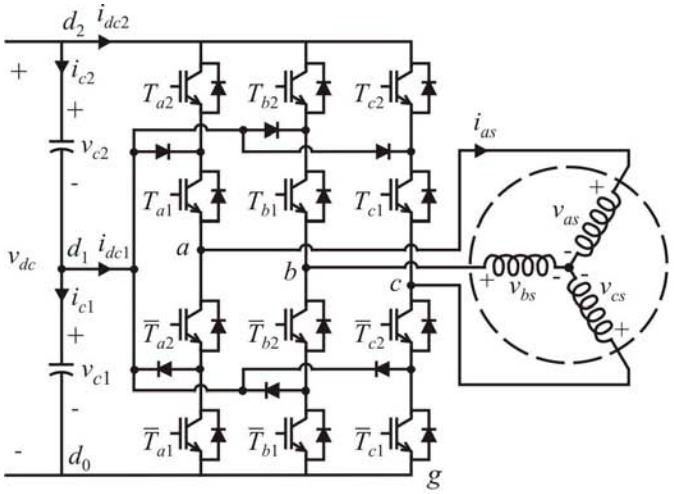

Figure 3.2-1. Three-level diode-clamped inverter topology.

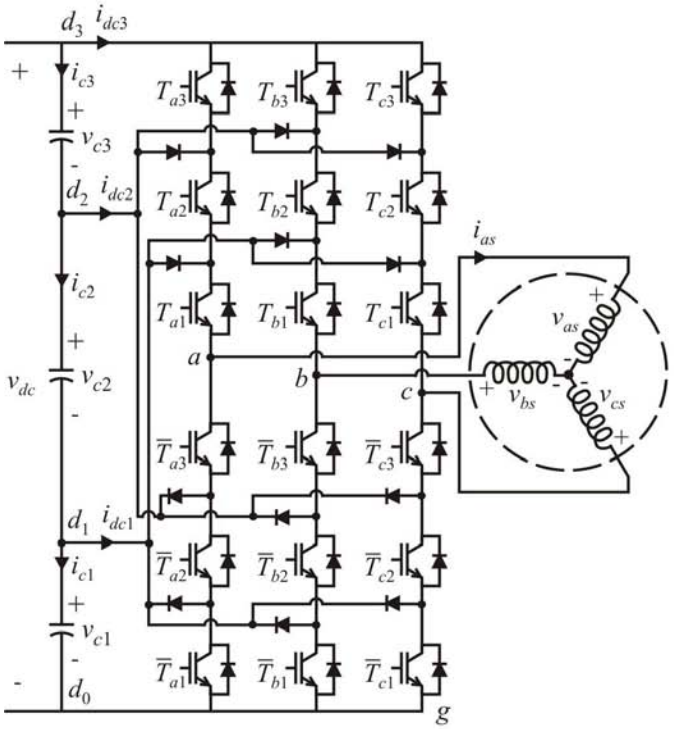

Figure 3.2-2. Four-level diode-clamped inverter topology.

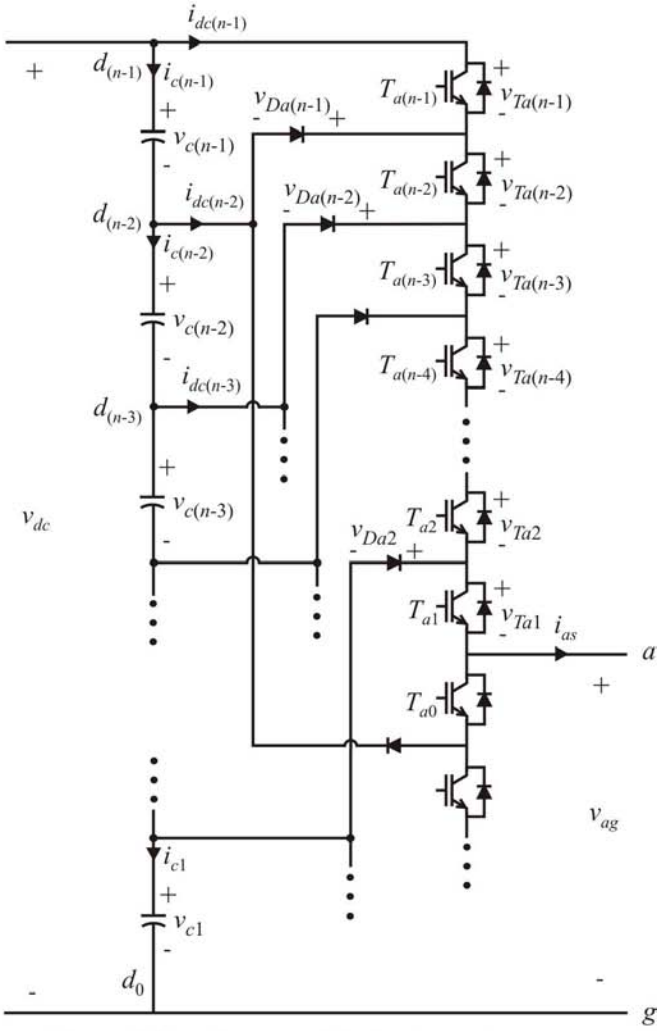

Figure 3.2-3. The *n*-level diode-clamped inverter.

3.2.2 Flying capacitor structure

Another fundamental multilevel topology, the flying capacitor, involves series connection of capacitor clamped switching cells [5]. This topology has several unique and attractive features when compared to the diode-clamped inverter. One feature is that added clamping diodes are not needed. Furthermore, the flying capacitor inverter has switching redundancy within the phase which can be used to balance the flying capacitors so that only one dc source is needed.

Figure 3.2-4 shows the three-level flying capacitor inverter. The general concept of operation is that each flying capacitor is charged to one-half of the dc voltage and can be connected in series with the phase to add or subtract this voltage. Table 3.2-3 shows the relationships for the *a*-phase

Table 3.2-3. Three-level flying capacitor relationships.

s_a	T_{a2}	T_{a1}	v_{ag}	i_{ac1}	i_{adc}
0	0	0	0	0	0
1	0	1	v_{ac1}	$-i_{as}$	0
	1	0	$v_{dc} - v_{ac1}$	i_{as}	i_{as}
2	1	1	v_{dc}	0	i_{as}

In comparison to the three-level diode-clamped inverter, an extra switching state is possible. In particular, there are two transistor states which make up the level $s_a = 1$. Considering the direction of the *a*-phase flying capacitor current i_{ac1} for the redundant states, a decision can be made to charge or discharge the capacitor and therefore, the capacitor voltage can be regulated to its desired value by switching within the phase. In Table 3.2-3, the current i_{adc} is the *a*-phase component of the dc current. The total dc current can be calculated by summing the components for all phases.

Figure 3.2-5 shows the structure for the *a*-phase of the four-level flying capacitor inverter. For this inverter, the capacitors v_{ac1} and v_{ac2} are ideally charged to one-third and two-thirds of the dc voltage respectively. The four voltage levels are obtained by the relationships shown in Table 3.2-4.

Table 3.2-4. Four-level flying capacitor relationships.

s_a	T_{a3}	T_{a2}	T_{a1}	v_{ag}	i_{ac1}	i_{ac2}	i_{adc}
0	0	0	0	0	0	0	0
1	0	0	1	v_{ac1}	$-i_{as}$	0	0
	0	1	0	$v_{ac2} - v_{ac1}$	i_{as}	$-i_{as}$	0
	1	0	0	$v_{dc} - v_{ac2}$	0	i_{as}	i_{as}
2	0	1	1	v_{ac2}	0	$-i_{as}$	0
	1	1	0	$v_{dc} - v_{ac1}$	i_{as}	0	i_{as}
	1	0	1	$v_{dc} - v_{ac12} + v_{ac1}$	$-i_{as}$	i_{as}	i_{as}
3	1	1	1	v_{dc}	0	0	i_{as}

As with the three-level flying capacitor inverter, the highest and lowest switching states do not change the charge of the capacitors. The two intermediate voltage levels contain enough redundant states that both capacitors can be regulated to their ideal voltages.

For the general *n*-level flying capacitor inverter shown in Figure 3.2-6, the transistor voltages can be determined from the transistor signals by

$$\begin{aligned} v_{Tai} = \; & (1-T_{ai})\left[v_{aci} - v_{ac(i-1)} - I_a v_{sw} + (1-I_a)v_d\right] \\ & + T_{ai}\left[I_a v_{sw} - (1-I_a)v_d\right] \end{aligned} \tag{3.2-13}$$

When employing (3.2-13), the lowest and highest capacitor voltages will be $v_{ac0} = 0$ and $v_{ac(n-1)} = v_{dc}$. The transistor and diode currents can be calculated using

$$i_{Tai} = T_{ai} I_a i_{as} \tag{3.2-14}$$

$$i_{DTai} = T_{ai}(1-I_a) i_{as} \tag{3.2-15}$$

The capacitor currents can be calculated based on KCL equations as

$$i_{aci} = i_{Ta(i+1)} - i_{Tai} \tag{3.2-16}$$

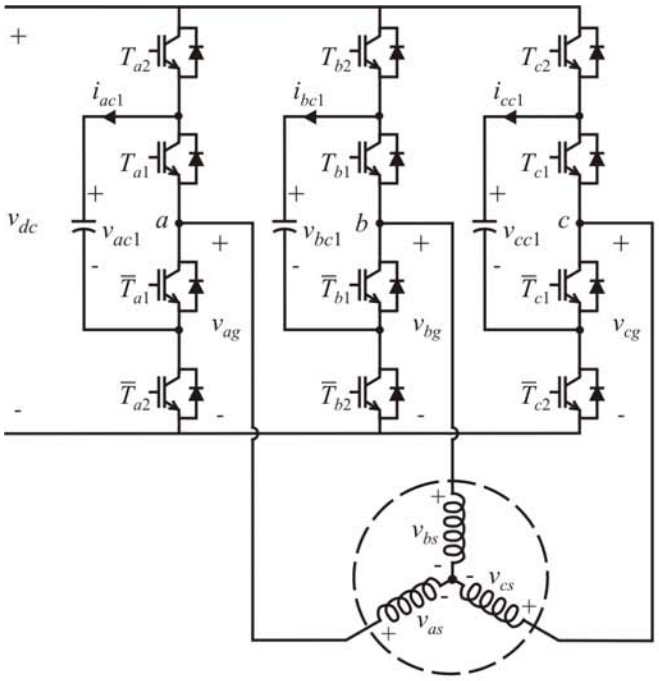

Figure 3.2-4. Three-level flying capacitor topology.

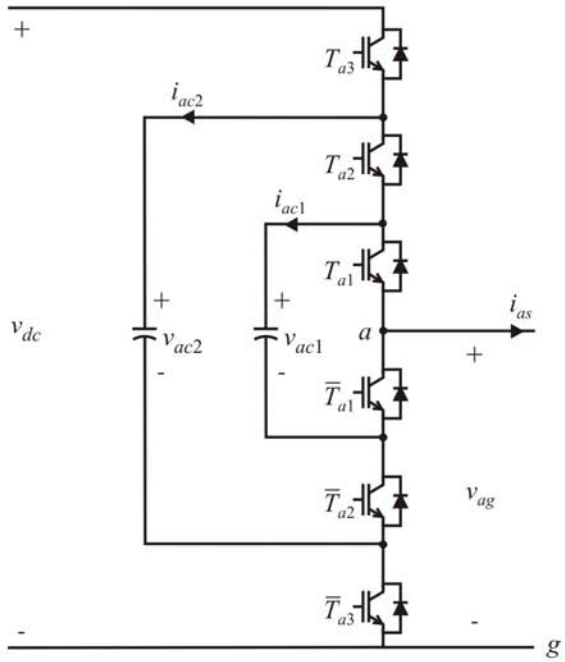

Figure 3.2-5. Four-level flying capacitor topology (*a*-phase).

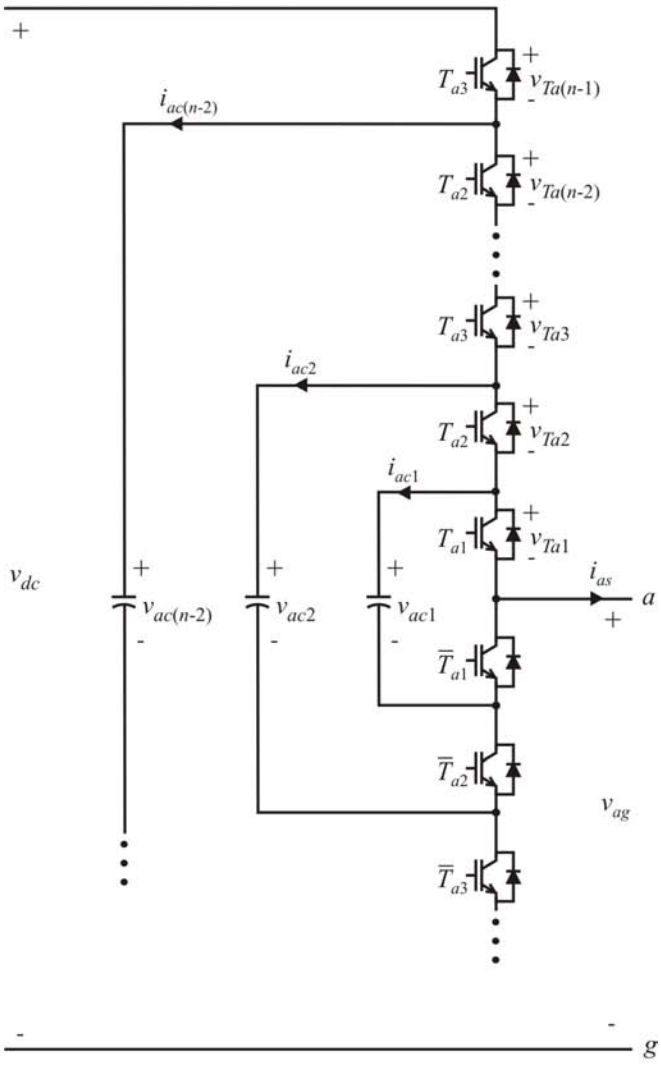

Figure 3.2-6. The generalized *n*-level flying capacitor inverter.

3.2.3 Series H-bridge multilevel inverter

The series H-bridge inverter appeared in 1975 [1], but several recent patents have been obtained for this topology as well [22-24]. Since this topology consist of series power conversion cells, the voltage and power level may be easily scaled. An apparent disadvantage of this topology is the large number of isolated voltages required to supply each cell. However, the cells can be supplied by phase-shifted transformers in medium-voltage systems in order to provide high power quality at the utility connection [22].

A two-cell series H-bridge inverter is shown in Figure 3.2-7. The inverter consist of familiar H-bridge (sometimes referred to as full-bridge) cells in a cascade connection. Since each cell can provide three voltage levels (zero, positive dc voltage, and negative dc voltage), the cells are themselves multilevel inverters. Taking the *a*-phase for example, the relationship for a particular cell can be expressed as in Table 3.2-5.

Table 3.2-5. H-bridge cell relationships.

s_{aHi}	T_{aLi}	T_{aRi}	v_{agi}	i_{adci}
-1	0	1	$-v_{adci}$	$-i_{as}$
0	0	0	0	0
	1	1	0	0
1	1	0	v_{adci}	i_{as}

Since the H-bridge cells can supply both positive and negative voltages contributing to the line-to-ground voltage, a switching state is defined for H-bridge cells s_{aHi} that has negative values. From Table 3.2-5, it can be seen that the general relationships for cell *i* are

$$v_{agi} = (T_{aLi} - T_{aRi})v_{dci} \tag{3.2-17}$$

$$i_{adci} = (T_{aLi} - T_{aRi})i_{as} \tag{3.2-18}$$

In addition, the per-cell switching state may be expressed in terms of the transistor signals by

$$s_{aHi} = T_{aLi} - T_{aRi} - 1 \tag{3.2-19}$$

Typically, the inverse relationship of (3.2-19) is needed since a multilevel modulator will determine the switching state. Due to the redundancy shown in Table 3.2-5, there is no unique way to obtain transistor signals from the switching state. However, solutions can be obtained by either ignoring some redundant states or

selecting redundant states to meet a particular goal (such as evenly distributing transistor switching losses or dc source currents [19]). The *a*-phase line-to-ground voltage may be expressed as the sum of the series cells or

$$v_{ag} = \sum_{i=1}^{p} v_{agi} \tag{3.2-20}$$

for *p* series power cells.

In the first implementations of the series H-bridge inverter, the isolated dc sources were equal leading to an overall switching state of

$$s_{aH} = \sum_{i=1}^{p} s_{aHi} \tag{3.2-21}$$

In this case, the general formula (3.1-1) can be used for calculation of the line-to-ground voltages with s_{aH} in place of s_a and likewise for the *b*- and *c*-phases.

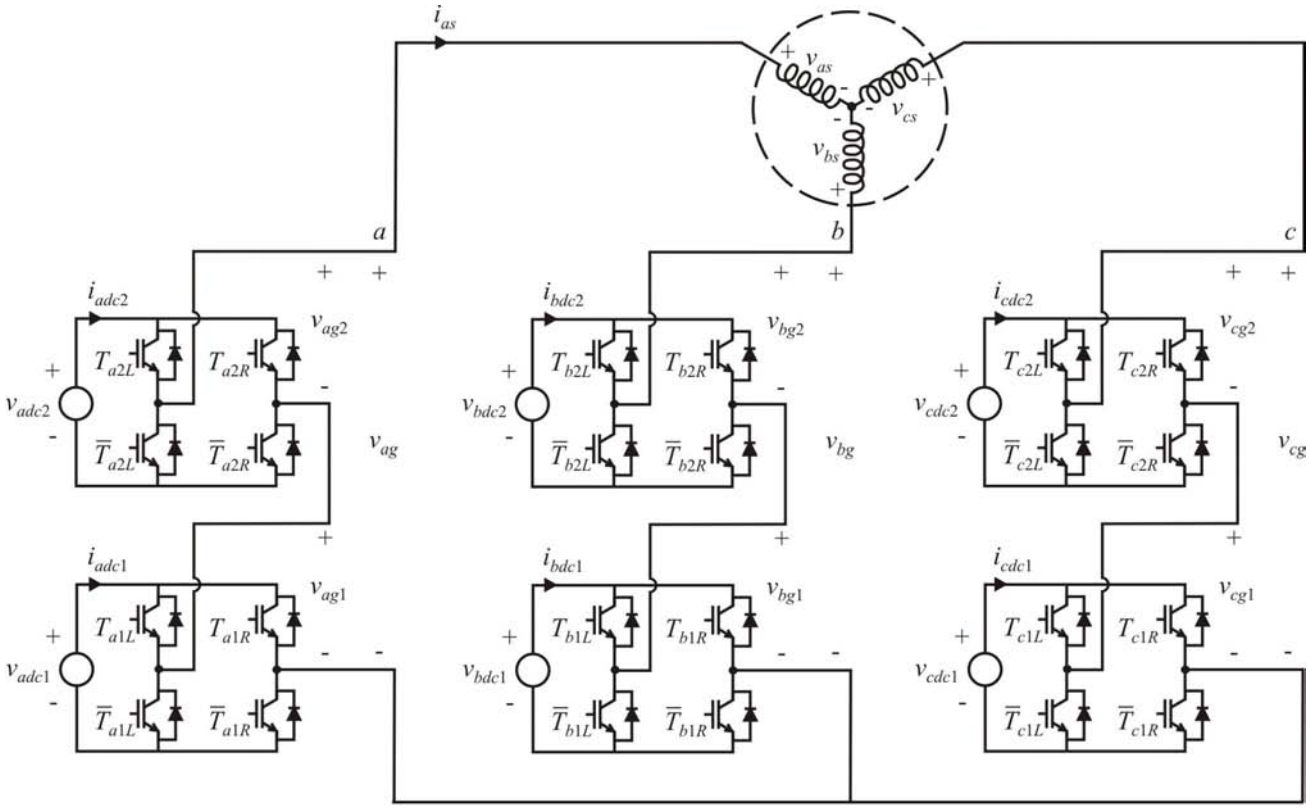

Figure 3.2-7. The two-cell series H-bridge drive.

3.2.4 Parallel phase topology

Since nearly all multilevel inverters involve effective series connection of transistor devices, parallel connection of inverter poles through inter-phase reactors is sometimes overlooked or not recognized as a multilevel solution. However, the multilevel features and redundancy were noted by researchers some time ago [6]. One advantage of parallel connection is that the devices share current and this topology is good for high current loads. It is also reasonable to perform parallel combinations of diode-clamped poles so that the transistor voltage and current ratings are reduced [7]. This structure has the advantage of providing a high number of voltage levels while reducing the voltage and current stress on the individual transistors.

Figure 3.2-8 shows a three-phase three-level inverter made from parallel two-level poles. The inter-phase reactor is similar to a typical transformer with the exception that an air-gap exists in the core to ensure linearity and the windings are such that the resistance and leakage inductances are small. With these assumptions, the reactor will have equal voltages on each half meaning that the line-to-ground voltage is the average of that of each of the two-level poles. Then the general relationships for the *a*-phase can be listed as in Table 3.2-6.

Table 3.2-6. Parallel inverter relationships.

s_a	T_{aL}	T_{aR}	v_{ag}	i_{adc}
0	0	0	0	0
1	0	1	$v_{dc}/2$	i_{asR}
	1	0	$v_{dc}/2$	i_{asL}
2	1	1	v_{dc}	i_{as}

The *a*-phase line-to-ground voltage can be expressed in terms of the transistor signals by

$$v_{ag} = \frac{1}{2}(T_{aL} + T_{aR})v_{dc} \tag{3.2-22}$$

For ideal operation, the reactor currents should be equal $i_{asR} = i_{asL}$. In practice, this is easy to ensure since the redundant states can be selected to drive the differential mode reactor current to zero. To understand the operation of the inter-phase reactor, it can be replaced by the model shown in Figure 3.2-9. This model is derived from the standard transformer model [27] with the resistance and leakage inductance set to zero. As it turns out, the transformer model is better suited for the reactor since the reactor contains an air-gap yielding negligible core losses. The 1:1 transformers in Figure 3.2-9 are ideal and thus ensure that each side of the reactor will have the same

voltage. This magnetizing voltage can be expressed in terms of the transistor signals and dc voltage as

$$v_{am} = \frac{1}{2}(T_{aL} - T_{aR})v_{dc} \tag{3.2-23}$$

From (3.2-23), the magnetizing current can be calculated by

$$p\,i_{am} = \frac{v_{am}}{L_m} \tag{3.2-24}$$

Once the magnetizing current is known, the left and right reactor currents can be found by solving the two unknowns from the two KCL equations

$$i_{asL} - i_{asR} = i_{am} \tag{3.2-25}$$

$$i_{asL} + i_{asR} = i_{as} \tag{3.2-26}$$

Considering (3.2-23), it can be seen that the redundant states in Table 3.2-6 can make the magnetizing voltage positive or negative effecting the change in i_{am} according to (3.2-24). This can be used to control i_{am} to zero yielding zero differential mode current according to (3.2-25) so that $i_{asR} = i_{asL}$.

It should be pointed out that the material presented herein shows the fundamental example. Extensions of this material include paralleling multi-level phases [7], combining the parallel topology with an H-bridge structure [28], and paralleling more than two phases.

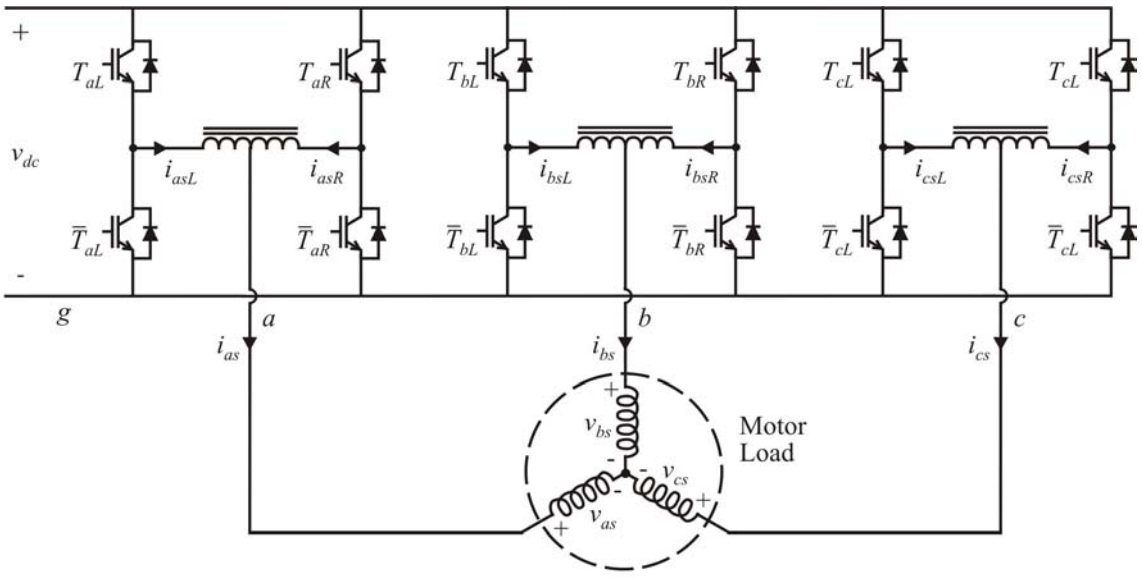

Figure 3.2-8. Parallel phase inverter..

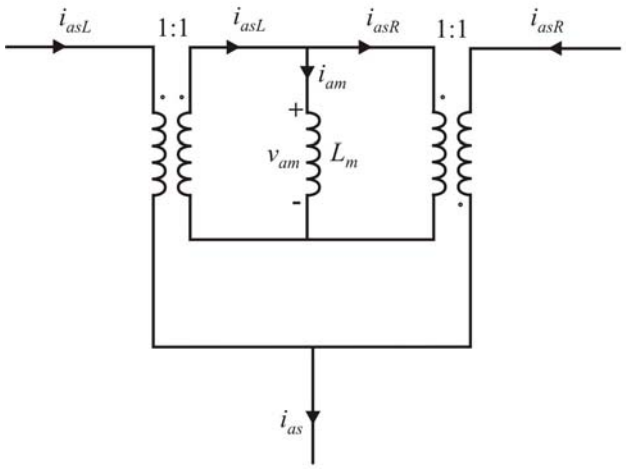

Figure 3.2-9. Model of the inter-phase reactor.

3.3 MULTILEVEL MODULATION

One first impression of a multilevel power converter is that the large number of switches may lead to complex pulse-width modulation (PWM) switching algorithms. However, early developments in this area demonstrated the relatively straightforward nature of multilevel PWM. This section presents the fundamental methods as well as reviews some novel research that has appeared in the literature. The methods are divided into the traditional voltage-source and current-regulated methods. An advantage of the current-regulated methods is that there is a need to control the current directly since the higher-level control (vector control, reactive power control, active rectifier, etc.) nearly always outputs commanded currents. However, current controls typically depend on event scheduling and are therefore analog implementations which can only be reliably operated up to a certain power level. Some discrete current-regulated methods are presented herein, but due to their nature, the harmonic performance is not as good as that of voltage-source methods. Voltage-source methods also more easily lend themselves to digital signal processor (DSP) or programmable logic device (PLD) implementation.

3.3.1 Voltage-source methods

The development of voltage-source modulation has taken two major paths; sine-triangle modulation in the time domain and space vector modulation in the *q*-*d* stationary reference frame. It was pointed out early on in PWM development that sine-triangle and space vector modulation are exactly equivalent in every way [29]. This equivalence has also been shown for the three-level inverter [30]. Adjusting some parameters in the sine-triangle scheme (such as the triangle shape and sine-wave harmonics) is equivalent to adjusting other parameters in the space vector scheme (such as the switching sequence and dwell time). In the two-level system, the adjustment of these parameters has been studied extensively [31] and a general tradeoff between harmonics and switching losses has been identified [31,32]. The same type of analysis is now being studied for multilevel inverters [33-35].

This section presents an overview of the sine-triangle and space vector methods. Discrete implementation on a DSP is also discussed. As it turns out, for DSP implementation, there is no need to define triangle waveforms or voltage vectors. In addition to the fundamental schemes, a novel scheme based on the minimum distance to the nearest voltage vector is also reviewed [36].

Based on the general equation (3.1-1), the inverter line-to-ground voltage can be directly controlled through the switching state. For a specific inverter, the switching state is broken out into transistor signals as described in the sections above. However, as a control objective, it is more desirable to regulate the line-to-neutral voltages of the load. According to (3.1-2), it can be concluded that there is an

infinite set of line-to-ground voltages for a desired set of line-to-neutral voltages since the matrix has a zero determinate. This provides some flexibility in the line-to-ground voltages since any common-mode terms included will not appear on the load. In a three-phase system, the common terms include dc offset and any triplen harmonics. To narrow the possibilities, the commanded line-to-ground voltages will be defined herein as

$$\begin{bmatrix} v_{ag}^{*} \\ v_{bg}^{*} \\ v_{cg}^{*} \end{bmatrix} = \frac{m v_{dc}}{2} \begin{bmatrix} \cos(\theta_c) \\ \cos\left(\theta_c - \frac{2\pi}{3}\right) \\ \cos\left(\theta_c + \frac{2\pi}{3}\right) \end{bmatrix} + \frac{v_{dc}}{2} \left[1 - \frac{m}{6} \cos(3\theta_c) \right] \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \tag{3.3-1}$$

where *m* is the modulation index which has a range of

$$0 \le m \le \frac{2}{\sqrt{3}} \tag{3.3-2}$$

and θ_c is the converter electrical angle. In (3.3-1), the first set of terms on the right hand side define a sinusoidal set of commanded voltages with controllable amplitude and frequency through *m* and θ_c respectively. The second set of terms on the right hand side are the common-mode terms. In this case, a dc offset is applied so that the commanded line-to-ground voltages will be within the allowable range of zero to the dc voltage. The other common-mode term is a third harmonic component which is added to fully utilize the dc source voltage [27]. The common-mode terms of (3.3-1) are just the minimum set and it is possible to command other types of line-to-ground voltages, including discontinuous waveforms, in order to optimize switching frequency or harmonics [31,33].

Some fundamental definitions will now be presented for reference when describing the modulation methods. First, duty cycles are defined by scaling the commanded voltages with modifications to account for multiple voltage levels. The modified duty cycles are

$$\begin{bmatrix} d_{am} \\ d_{bm} \\ d_{cm} \end{bmatrix} = \left(\frac{n-1}{2} \right) \begin{bmatrix} m\cos(\theta_c) \\ m\cos\left(\theta_c - \frac{2\pi}{3}\right) \\ m\cos\left(\theta_c + \frac{2\pi}{3}\right) \end{bmatrix} + \left(\frac{n-1}{2} \right) \left[1 - \frac{m}{6} \cos(3\theta_c) \right] \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \tag{3.3-3}$$

Next, a commanded voltage vector is defined by

$$v_{qds}^{s*} = v_{qs}^{s*} - j\, v_{ds}^{s*} \tag{3.3-4}$$

where the commanded *q*- and *d*-axis voltages are related to the *a*-*b*-*c* variables of (3.3-1) by [27]

$$v_{qs}^{s*} = \frac{2}{3}v_{ag}^{*} - \frac{1}{3}v_{bg}^{*} - \frac{1}{3}v_{cg}^{*} \tag{3.3-5}$$

$$v_{ds}^{s*} = \frac{1}{\sqrt{3}}\left(v_{cg}^{*} - v_{bg}^{*}\right) \tag{3.3-6}$$

It should be pointed out that the commanded *q*- and *d*-axis voltages can also be defined in terms of desired line-to-neutral voltages since the zero sequence is being ignored.

3.3.1.1 Sine-triangle modulation

One of the most straightforward methods of describing voltage-source modulation is to illustrate the intersection of a modulating signal (duty cycle) with triangle waveforms. Figure 3.3-1 demonstrates the sine-triangle method for a nine-level inverter. Therein, the *a*-phase duty cycle is compared with eight (*n*-1 in general) triangle waveforms. The switching rules are simply

$$s_{ai} = \begin{cases} 1 & d_{am} > tri \\ 0 & \text{elsewise} \end{cases} \tag{3.3-7}$$

$$s_a = \sum_{i=1}^{n-1} s_{ai} \tag{3.3-8}$$

In summary, the switching state is the number of triangle waveforms below the modified duty cycle. The *b*- and *c*-phase duty cycles are compared to the same set of triangle waveforms to create respective switching states.

Much work has been done in the area of analyzing the harmonics generated by multilevel sine-triangle modulation [33-35] and obtaining closed form expressions. Other research has focused on utilizing different frequencies for some of the carrier triangle waveforms in order to improve the efficiency and switch utilization of the standard diode-clamped topology [37]. Another recent innovation involves shifting the boundary of the triangle waveforms in the three-level inverter in order to balance the capacitor voltages [38].

3.3.1.2 Space vector modulation

Space vector modulation (SVM) is based on vector selection in the *q-d* stationary reference frame. As an example, consider the commanded voltage vector defined by (3.3-4). For a four-level system, the commanded vector is plotted along with the vectors obtainable by the inverter in Figure 3.3-2. The desired vector v_{qds}^{s*} is shown at some point in time, but will follow the circular path if a three-phase set of voltages are required on the load. Although the circular path shown in the figure, the path may be arbitrary. The first step in the SVM scheme is to identify the three nearest vectors. In this example, they are v_{52}, v_{56}, and the redundant vectors v_{36} and v_{57}. The next step is to determine the amount of time that must be spent at each vector in order for the average voltage to be equal to the commanded voltage. This can be done using some simple mathematical relationships. In particular, the vectors and their corresponding times are related by

$$v_{36,57}T_{36,57} + v_{52}T_{52} + v_{56}T_{56} = v_{qds}^{s*}T_{sw} \tag{3.3-9}$$

where T_{sw} is the switching time of the PWM control which is the total of the time spent at each vector or

$$T_{sw} = T_{36,57} + T_{52} + T_{56} \tag{3.3-10}$$

Based on (3.3-9) and (3.3-10), the amount of time for each voltage vector can be computed by solving the inverse problem

$$\begin{bmatrix} \mathrm{Re}\{v_{36,57}\} & \mathrm{Re}\{v_{52}\} & \mathrm{Re}\{v_{56}\} \\ \mathrm{Im}\{v_{36,57}\} & \mathrm{Im}\{v_{52}\} & \mathrm{Im}\{v_{56}\} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} T_{36,57} \\ T_{52} \\ T_{56} \end{bmatrix} = \begin{bmatrix} \mathrm{Re}\{v_{qds}^{s*}\} \\ \mathrm{Im}\{v_{qds}^{s*}\} \\ T_{sw} \end{bmatrix} \tag{3.3-11}$$

The final step in the SVM scheme is to determine a sequence of switching for the voltage vectors. For this example, the switching sequence could be from v_{57} to v_{56} to v_{52} to v_{36}. At the end of the sequence, the controller switching time T_{sw} has elapsed and the process is repeated with updating the commanded voltage, identifying the three nearest vectors, calculating the switching times, and scheduling the switching sequence.

As can be seen, there are allot of free parameters in this process. The time spent at vectors v_{56} and v_{52} (sometimes called dwell time) is directly determined by (3.3-11), but the time spent at vectors v_{57} and v_{36} is an arbitrary split of $T_{36,57}$. Whether this time is split evenly or as a function of the commanded voltage angle can have an

effect on the inverter harmonics and switching losses. Instead of splitting the time, the sequence could be changed to switch from v_{57} to v_{56} to v_{52} which would reduce commutation. the sequence can also be reversed by switching from v_{52} to v_{56} to v_{57} which will affect the harmonics.

3.3.1.3 Discrete implementation

One attractive feature of voltage-source PWM methods is that they can be readily implemented on a DSP/PLD control. Figure 3.3-3 demonstrates a per-phase time-domain method of implementing PWM in a discrete time system for a four-level inverter. Therein, the modified *a*-phase duty cycle is shown along with the switching state output of the modulator. At each point in time, the *a*-phase duty cycle is updated based on the magnitude and phase of the commanded voltages in accordance with (3.3-3). The continuous calculation is shown in Figure 3.3-2 and is a small portion of the duty cycle shown in Figure 3.3-1. In a DSP system, discrete values of the duty cycle are computed which are represented by points in Figure 3.3-3. This creates a zero-order-hold effect which is negligible if the switching frequency is large compared to the changes in the duty cycle. In order to schedule the switching state transitions during the switching period, the nearest lower and upper voltage levels are determined. This is a simple matter of intergerizing the duty cycle using

$$ll_a = \mathrm{INT}(d_{am}) \tag{3.3-12}$$

$$ul_a = ll_a + 1 \tag{3.3-13}$$

where INT is the intergerization function that returns the nearest integer less than or equal to its argument. Next, a switching time for each *a*-phase is determined based on the proximity to the lower level by direct calculations. For the *a*-phase, this is calculated by

$$t_a = (d_{am} - ll_a)T_{sw} \tag{3.3-14}$$

As can be seen, the switching time t_a will range from zero to 100% of the switching period and is the time that should be spent at the upper level. The final step is scheduling the switching transitions. In Figure 3.3-3, the pulse is left-justified in the switching period starting at the upper level and transitioning to the lower level. The scheduling rules for this type of justification are

$$s_a = \begin{cases} ul_a & 0 \le t' \le t_a \\ ll_a & t_a < t' \le T_{sw} \end{cases} \tag{3.3-15}$$

where t' is time that is zero at the beginning of the switching period. The same procedure is applied to the *b*- and *c*-phases.

Usually, the nearest levels and switching times for each phase are calculated in a DSP. This information is then transferred to a PLD which operates at a higher a higher clock frequency and can make the transitions of the switching state on a nanosecond time scale. In a practical implementation, the DSP and PLD clocks are tied together by a PLD circuit which divides its clock and sends a clock signal to the DSP on the microsecond time scale. Exact details of this process can be found in the literature [39,40]. Besides the zero-order hold effect, there is a one-sample delay effect which is caused by the fact that the DSP will take some time to determine the levels and switching times. This effect is not shown in Figure 3.3-3, but the computed duty cycle (indicated by the discrete points) is used in the following switching period causing a lag between the duty cycle and the switching state. This effect is negligible for high switching frequencies.

Some comments are appropriate at this time to show the equivalence between the discrete implementation and the sine-triangle and SVM methods. The example shown in Figure 3.3-3 assumed that the switching state would start in the upper level and transition to the lower level at the appropriate time. An identical switching pattern is obtained in the sine-triangle method by using a saw-tooth waveform instead of a triangle waveform as shown in Figure 3.3-1. Likewise, moving the pulses to the right side of the switching period (a transition from the lower level to the upper level) would be equivalent to using a reverse saw-tooth waveform. If the pulses are centered within the switching period, then the result is the same as that using a triangle waveform. Since the sine-triangle and discrete methods are both performed on a per-phase basis and in the time domain, their equivalence is easily understood. The equivalence to SVM can be seen by creating a plot of the switching states for all three phases as shown in Figure 3.3-4. Therein the switching for a four-level inverter is shown over one switching period. In this example, the *c*-phase switches from level 1 to 0 with the shortest switching time (lowest duty cycle). The *b*-phase switches from 2 to 1 with an intermediate time representing a duty cycle greater than the *c*-phase. The *a*-phase switches from level 3 to 2 with the highest duty cycle. The result of switching the three phases is that four windows are created by the switching boundaries. The first window (where $s_a = 3$, $s_b = 2$, and $s_c = 1$) creates vector v_{57} according to (3.1-1) to (3.1-7). The next three windows create vectors v_{56}, v_{52}, and v_{36}. These are the same three nearest vectors in the example used in the section on SVM. The sequence is also the same. However, the sequence can be reversed in the discrete implementation by switching to right justification. In a similar way, the sequence can be reversed in the SVM method. There is much more to the equivalence of these methods including adding harmonics to the duty cycles in the sine-triangle method or changing the dwell times in the SVM method. For more details and mathematical relationships, the interested reader is referred to [29,30,41].

It can be seen that the discrete method presented herein relies on computation directly from the duty cycles and therefore it is not necessary to define triangle waveforms or voltage vectors. However, sine-triangle modulation is useful in that it can provide a straightforward method of describing multilevel modulation. Also, the SVM method leads to an insightful (and sometimes simpler) way to view the operation of multilevel inverters.

3.3.1.4 Space vector control

A rather unique voltage-source modulation method called space vector control (SVC) has been recently introduced [36]. Since it is fundamentally different than sine-triangle or SVM, it is presented in this separate section. The premise of this scheme is that the inverter can be switched to the vector nearest the commanded voltage vector and held there until the next cycle of the DSP [36]. Figure 3.3-5 illustrates the concept in the vector domain for an eleven-level inverter. Therein, only one quadrant of the vector plot is shown. The nearest vector to the commanded voltages is determined according to the hexagonal regions around each vector (some of which are shown in Figure 3.3-5). This operation is performed at each sample period of the DSP resulting in a simple modulation method. Since the vector is held for the DSP cycle, there is no need to compute switching times and schedule timing in the PLD.

Although this method is simple to implement, it is most useful on inverters with a relatively high number of voltage vectors. An example is the eleven-level series H-bridge inverter with five cells [36]. Another aspect of this control is that the DSP switching period should be small since the voltage is held constant for the entire switching time. Implementation of this scheme on an eleven-level inverter has shown that it can produce a lower THD than the SVM method [36].

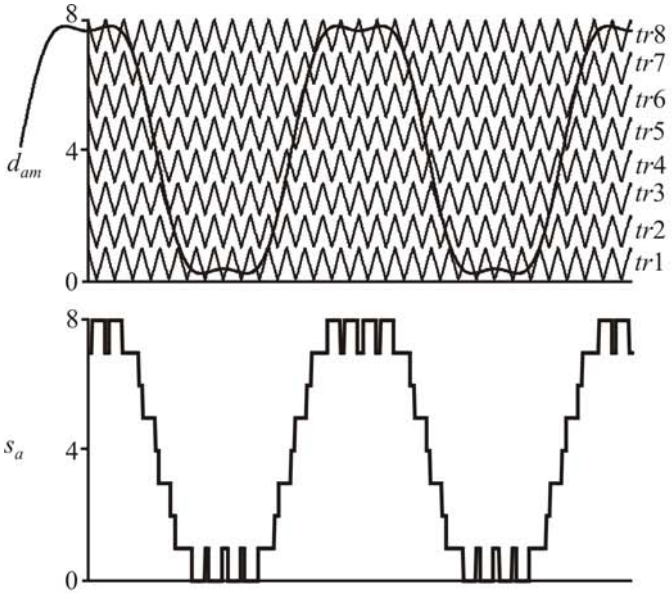

Figure 3.3-1. Nine-level sine-triangle modulation.

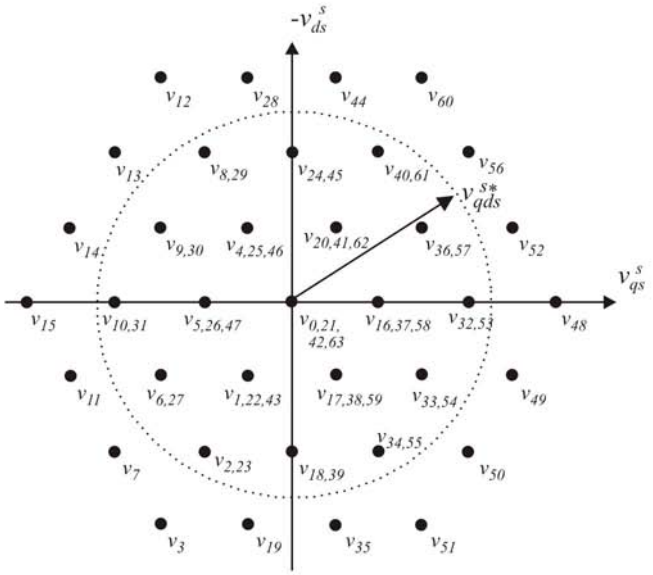

Figure 3.3-2. Four-level inverter space-vector modulation.

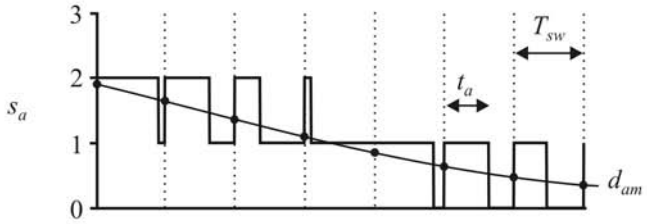

Figure 3.3-3. Per-phase discrete modulation.

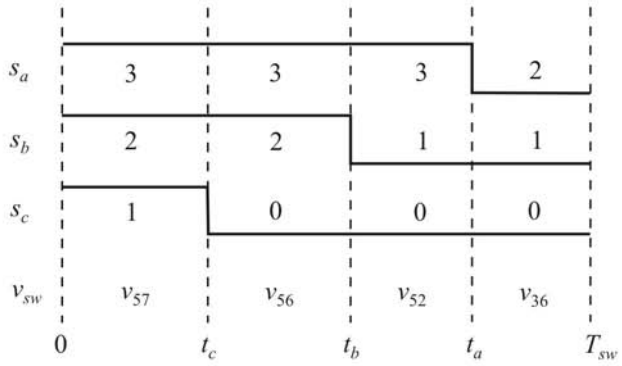

Figure 3.3-4. Duty-cycle modulation voltage vectors.

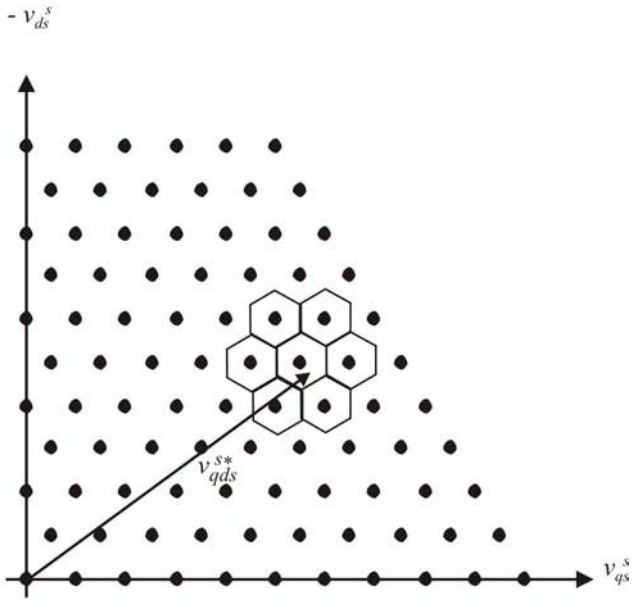

Figure 3.3-5. Eleven-level space vector control.

3.3.2 Current-regulated methods

This section presents an overview of the current-regulated PWM schemes. An extension of the two-level hysteresis control is presented. Although this method directly regulates the currents, it relies on an analog implementation which is not practical for higher power levels. As a compromise, two new methods, referred to as clocked sigma-delta and multilevel delta modulation, are introduced. These schemes provide a digital implementation, but have lower harmonic performance than the voltage source methods.

The tradeoff between discrete implementation and harmonic performance has been an issue for current-regulated controls. For two-level power conversion, some researchers have proposed predictive control [42] which relies on knowledge of the load parameters. Others have developed controls dependant on high-frequency timing of the current waveforms [43]. These methods and others have been applied to multilevel power conversion. The last part of this section mentions some of the alternate multilevel current-regulated approaches.

3.3.2.1 Hysteresis control

The hysteresis current-control concept typically employed in two-level drive systems [27] can be extended to multi-level systems by defining a number of hysteresis bands. This concept is illustrated in Figure 3.3-6 for the four-level inverter. The basic operation of the control involves defining n-1 evenly spaced hysteresis bands on each side of the commanded current. The voltage level is then increased by one each time the measured current departs from the commanded value and crosses a hysteresis band. One important detail of this control is that the voltage level will be at its highest or lowest value when the measured current crosses the lowermost or uppermost hysteresis band respectively. This ensures that the current will regulate about the commanded value. This straightforward extension of two-level current control results in good regulation of the currents and acceptable voltage level switching [44]. Furthermore, the multi-level hysteresis control handles steps changes in commanded current with a response similar to two-level hysteresis control.

There are many other methods of implementing hysteresis band based current controls for multilevel inverters. The amount of analog circuitry can be reduced by using a single hysteresis band and increasing or decreasing the voltage levels each time the current touches the band. This method is then coupled with timing and a voltage controlled oscillator to drive the current error to zero [45]. An extension to this method uses two hysteresis bands to provide better dynamic performance, but still utilize a small amount of analog circuitry for a large number of voltage levels [46]. The dual hysteresis band approach has also been used in the four-level diode-

clamped rectifier where the inner band is used to achieve capacitor voltage balancing and the outer band is used for current regulation [14].

3.3.2.2 Clocked sigma-delta modulation

Some current-regulated schemes are based on the sigma-delta function. As an example, the four-level sigma delta function is shown in Figure 3.3-7 for the *a*-phase. Based on the hysteresis level h, the per-phase switching state is determined from the current error. The function can be implemented directly with analog components or it can be implemented on a DSP based on a fixed clock frequency. In a two-level system, the hysteresis level is zero and the control reduces to that of standard delta modulation [47]. As with two-level systems, the switching frequency of the inverter may be less than the clock frequency since the voltage level may not change every time the control is clocked. The current tracking improves with increasing clock frequency, and a relatively high frequency is needed for good performance. This makes the control somewhat undesirable, although digital implementation is an advantage.

3.3.2.3 Multilevel delta modulation

The concept behind multilevel delta modulation is illustrated for the four-level system in Figure 3.3-8. As with clocked sigma delta modulation, the control operates on a per-phase basis and can be implemented on a DSP. The general scheme functions by increasing or decreasing the voltage level by one at each clock cycle of the DSP depending on whether the current error is positive or negative respectively. In this control, the hysteresis band does not need to be defined. In the two-level implementation, the control reduces to that of standard delta modulation [47]. As with clocked sigma-delta modulation, the clock frequency must be set relatively high in order to obtain good current tracking.

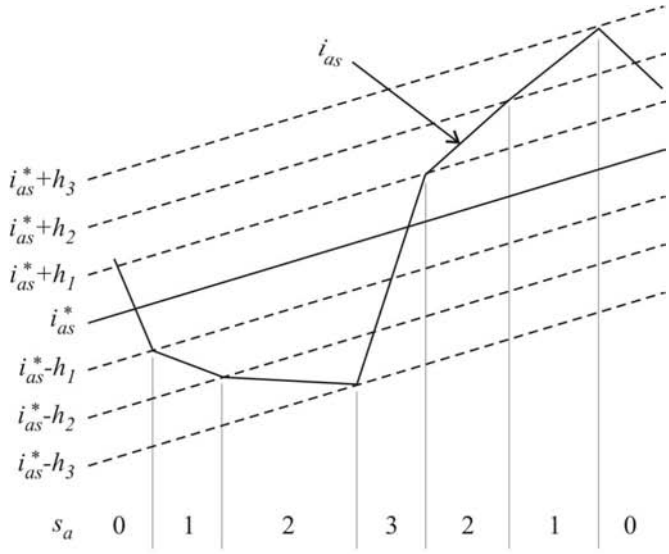

Figure 3.3-6. Illustration of hysteresis current control.

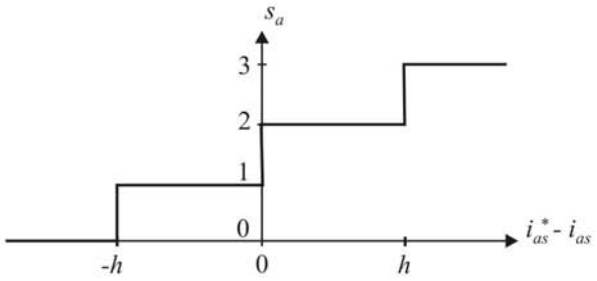

Figure 3.3-7. Four-level sigma-delta function.

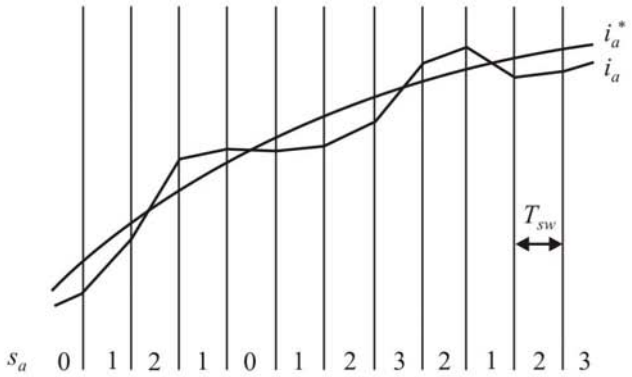

Figure 3.3-8. Four-level delta control scheme.

3.4 REDUNDANT STATE SELECTION

3.4.1 General concept and laboratory implementation

In previous sections, it was noted that some inverter switching states are redundant in that there are several combinations that produce the same output voltages. Therefore, the exact inverter switching is not unique and this redundancy may be utilized to achieve certain goals. Among the possible redundant state selection (RSS) goals are

- Capacitor voltage balancing
- Reactor current sharing
- DC source current control
- Switching frequency reduction

It is also important to point out that two types of redundancy are possible. Joint-phase RSS involves changing the common-mode voltage (that is increasing or decreasing the voltage level of all three phases). This was demonstrated in the first section during the discussion of voltage vectors. In the voltage vector plot, the joint-phase RSS can clearly be seen by the voltage vectors achievable by more than one combination of switching states. For a particular set of switching states, the number of redundant states using joint-phase redundancy is given by (3.1-11). Per-phase redundancy refers to certain inverter topologies which have redundant switching states within each phase. An example of this is the flying capacitor topology where several transistor switching combinations lead to the same line-to-ground voltage.

The fundamental theory of RSS is to use inverter equations and operating conditions to determine the best redundant state to meet particular goals. In order to implement this concept, digital flags are created which represent inverter operation (capacitor voltage balance, current direction, etc.). The digital flags along with the modulator desired switching state form the input to an RSS table which can be filled off-line based on the inverter equations [4]. Using this method, the best redundant state can be instantaneously selected during inverter operation.

Figure 3.4-1 shows a schematic of how the table can be included in a PLD. Based on the modified duty cycles, the DSP calculates the lower levels and switching times as described above. Many commercial DSPs have on-board PWM channels for two-level operation. These may be loaded with the switching times and their two-level outputs ($PWMa$, $PWMb$, and $PWMc$) can be added to the lower levels in the PLD section to produce the switching states. Using this method, it is not necessary to have a modulation channel for each transistor pair. The switching states at this stage are commanded by the modulator and are denoted s_a^*, s_b^*, and s_c^*. The

commanded switching sates are input to the RSS table in the PLD along with the digital flags. In Figure 3.4-1, the digital flags include I_a, I_b, and I_c which indicate the direction of the *a*- *b*- and *c*-phase currents as well as flags indicating over- or under-charge for the inverter capacitors. Some analog circuitry will be required in order to generate the digital flags. More specifics on the digital flags will be given later. For now, it should be considered that the digital flags represent the state of the system relative to the RSS goals. This information is latched by the PWM modulator so that the information is only updated at the beginning of a PWM cycle. This prevents the table inputs from changing in the middle of a PWM cycle. The RSS table output is the final set of switching states that are sent to the inverter. At the top of Figure 3.4-1, an example of the possible output is shown. This example is identical to the previous example shown in Figure 3.3-4. Therein, the last PWM window has been changed by the RSS table from ($s_a^* = 2$, $s_b^* = 1$, $s_c^* = 0$) to ($s_a = 3, s_b = 2, s_c = 1$). As can be seen, the RSS switching can have an impact on the switching frequency. Typically, an increase in switching frequency is necessary in order to satisfy the RSS goals. The outputs of the RSS table are input to a breakout table which produces the transistor signals for a particular topology from the switching state as described above. In systems involving per-phase RSS, it is necessary to absorb this table into the RSS table making the table output the transistor signals.

Figure 3.4-2 shows the implementation of an RSS table in the DSP. In this case, the level and timing information for all phases is used to determine commanded switching states for the four windows labeled I, II, III, and IV. The DSP then performs four table look-ups based on the commanded switching states. For the digital flags, the analog signals (currents and capacitor voltages for example) are read into the DSP. After digital filtering, the flags are calculated. The result is a switching state for each window which includes the RSS. This information and the switching times are transmitted to the PLD through digital outputs where the PWM is implemented.

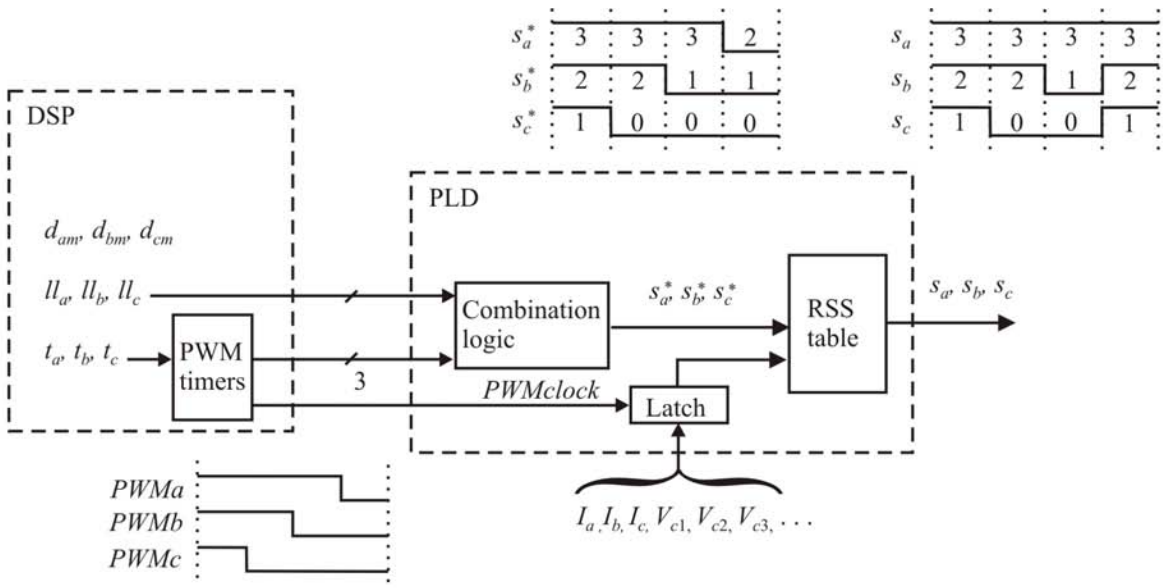

Figure 3.4-1. Redundant state selection (RSS) implemented in a PLD.

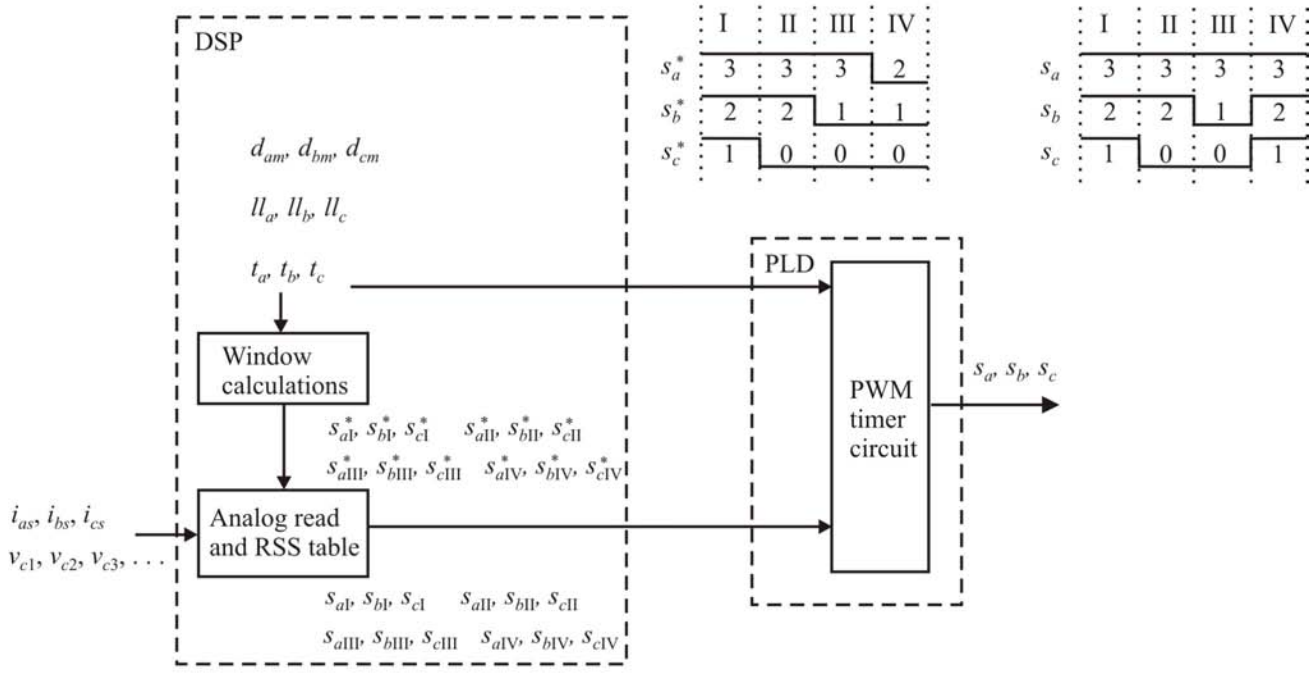

Figure 3.4-2. Redundant state selection (RSS) implemented in a DSP.

3.4.2 Capacitor voltage balancing

The four-level diode-clamped inverter of Figure 3.2-2 will be used to illustrate the use of RSS for capacitor voltage balancing. Since there is no per-phase redundancy in this system, joint-phase RSS will be utilized.

To use the general control structures of Figures 3.4-1 and 3.4-2 to specifically control a four-level inverter with the RSS goal of capacitor voltage balancing, the digital flags and table need to be defined. The current flags I_a, I_b, and I_c are one for positive and zero for negative values of i_{as}, i_{bs}, and i_{cs} respectively. Three digital flags indicating the capacitor voltage balance are defined by [4]

$$V_{c12} = \begin{cases} 1 & v_{c1} > v_{c2} \\ 0 & v_{c1} \le v_{c2} \end{cases} \tag{3.4-1}$$

$$V_{c23} = \begin{cases} 1 & v_{c2} > v_{c3} \\ 0 & v_{c2} \le v_{c3} \end{cases} \tag{3.4-2}$$

$$V_{c31} = \begin{cases} 1 & v_{c3} > v_{c1} \\ 0 & v_{c3} \le v_{c1} \end{cases} \tag{3.4-3}$$

Filling the RSS table is a matter of considering all of the possible table inputs off-line. For each set of switching states and digital flags, a state can be found which will reduce the capacitor voltage imbalance. For the four-level inverter with joint-phase redundancy, the switching states can be categorized into four cases. The case number for each switching state is defined as the number of capacitors that the switching state spans. Consider case 1 shown in Figure 3.4-3. In terms of commanded switching state, this case represents ($s_a^* = 2$, $s_b^* = 2$, $s_c^* = 1$). It can be shown from the capacitor differential equations that the dc source current does not affect the capacitor voltages [4] and in that case, the switching state has a direct impact on the voltage v_{c2} only. In particular, the load will discharge the capacitor if $I_c = 0$ and charge the capacitor if $I_c = 1$. According to 3.4-1, $n_{RSS} = 3$ and the other two redundant states can be found by increasing or decreasing the states of all three phases simultaneously leading to ($s_a^* = 3$, $s_b^* = 3$, $s_c^* = 2$) and ($s_a^* = 1$, $s_b^* = 1$, $s_c^* = 0$). For case 1, the best redundant state can be evaluated by noting whether the load current is charging or discharging and then selecting the state which places the load across the least charged or most charged capacitor respectively. The least or most charged capacitor can be determined from the information contained in (3.4-1) to (3.4-3). Figure 3.4-3 shows two examples for case 2. In case 2a, the load

connections span two capacitors with one phase connected to the center of the two. From the example, it can be seen that the *a*-phase current determines the change of v_{c3} and the *c*-phase current determines the change of v_{c2}. The redundant state can be found by decreasing the level of all phases by one. In that case, the voltages v_{c2} and v_{c1} will be affected by the *a*- and *c*-phase currents respectively. Choosing the best state case 2a is done with priority to improving the voltage balance of v_{c2}. This is due to a tendency of the center capacitor to become unbalanced in the four-level inverter [4,14]. However, it is possible that both redundant states have the same effect on the center capacitor. In that case, the next priority is to select the sate that improves v_{c1} or v_{c3}. Case 2b is defined as a switching state where the phase connections span two capacitors without a connection to the junction of those capacitors as shown in the example in Figure 3.4-3. In this example, the redundant state is found by decreasing the voltage levels of all phases by one. By considering the load currents, it can be seen that both redundant states have the same effect on the center capacitor. Therefore, for case 2b the best state is determined by the upper and lower capacitors. In the four-level inverter, there are also two additional cases. Case 0 where all phases are connected to the same capacitor junction. In this case, the load currents do not effect the capacitor voltages and therefore, the output of the RSS table is set equal to the input. In case 3, there are no redundant states and so the RSS table output is set to the input for those cases as well. Based on the input data to the table, there are a large number of states to consider. However, if they are categorized into four cases, the process can be automated in a subroutine which automatically considers all input states based on some general rules for the cases. The RSS table is then generated automatically in a program loop.

Figure 3.4-4 shows the diagram for a four-level rectifier / inverter system. Although the focus herein has been on inverter operation, the four-level rectifier topology is identical to that of the inverter [14,48]. Since the rectifier shares a bank of capacitors with the inverter and the definition of rectifier currents are out of the rectifier, the RSS table for the rectifier is identical to that of the inverter. A four-level hysteresis current control is used for the rectifier modulation. The outer loop dc voltage control regulates the total dc voltage and also synchronizes with the source voltage for unity power factor operation [48]. Figure 3.4-5 shows laboratory measurements of the line-to-line voltages and phase currents of the four-level system. In this study, the rectifier was supplied from a 420 V (line-to-line rms) source and the commanded dc voltage was 660 V (220 V on each capacitor). The inverter was driving an 18 kW induction motor at rated load. The inverter was controlled with discrete modulation with a fundamental component of 100 Hz, a modulation index of $m = 1.0$, and a DSP clock frequency of 10 kHz. The rectifier control was operating with an effective modulation index of 1.0 and was operating with a 60 Hz fundamental component (as depicted by the source). From the lab studies, it can be seen that there are seven distinct line-to-line voltages of the rectifier and inverter. Since the RSS held the capacitors at their desired values, the voltage levels appear as evenly spaced.

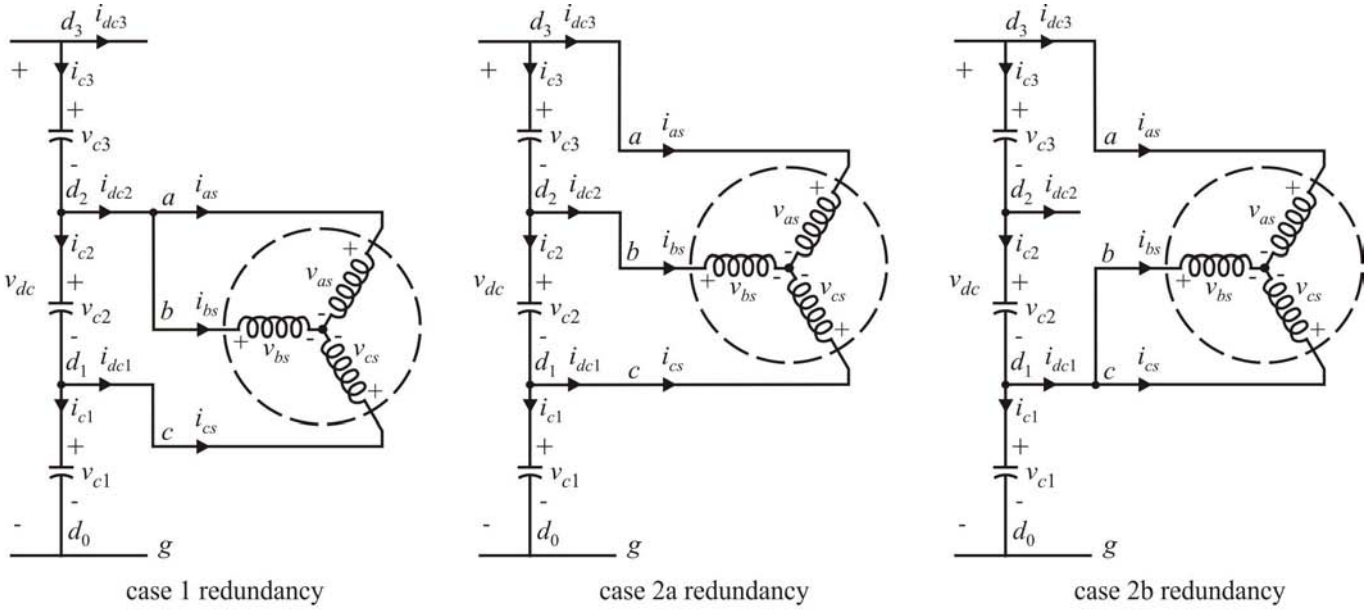

Figure 3.4-3. Four-level redundant state selection cases.

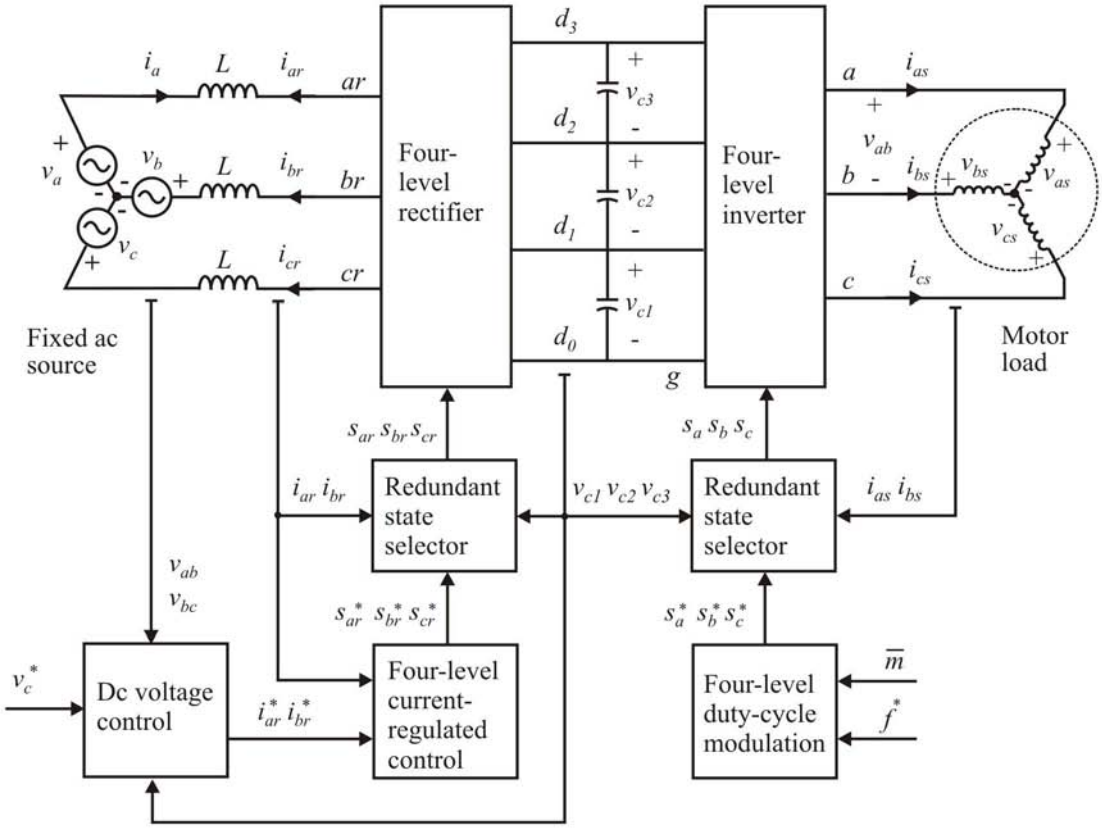

Figure 3.4-4. Four-level rectifier / inverter system.

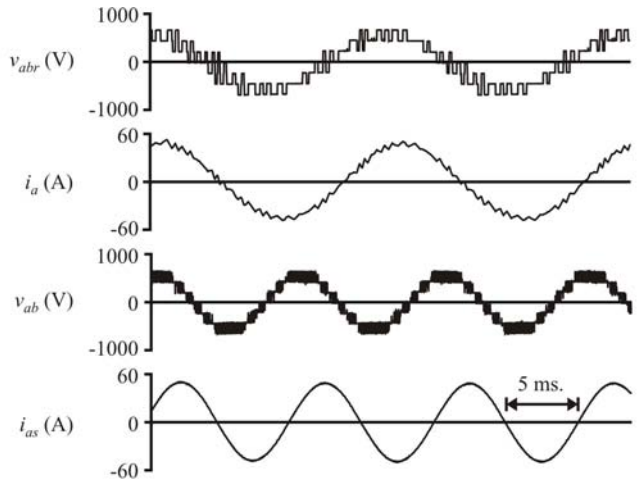

Figure 3.4-3. Four-level rectifier/inverter system performance.

3.4.3 Reactor current sharing

For the parallel topology shown in Figure 3.2-8, the redundant states can be used to ensure current sharing in the reactor. This application is an example of per-phase RSS where the control has the structure shown in Figure 3.4-4. The digital flag input for the *a*-phase is

$$I_{aLR} = \begin{cases} 1 & i_{asL} > i_{asR} \\ 0 & i_{asL} \le i_{asR} \end{cases} \tag{3.4-4}$$

Similar current sharing flags are defined for the *b*- and *c*-phase. In this topology, the lowest $s_a = 0$ and highest $s_a = 2$ switching states do not affect the reactor current balance. This is fortunate, since there is no redundancy available for these states. The middle state affects the reactor current sharing, but has redundancy according to Table 3.2-6. The redundant choice to be placed in the RSS table is straightforward according to the discussion in the previous section about the inter-phase reactor. Specifically, the transistors can be set to $T_{aR} = I_{aLR}$ and $T_{aL} = 1 - I_{aLR}$ when $s_a^* = 1$.

Figure 3.4-5 shows the three-level inverter simulated performance based on the RSS rules described above. The dc source voltage was 660 V and the inverter was controlled with voltage-source modulation using a fundamental frequency of 100 Hz, a switching frequency of 10 kHz, and a modulation index of $m = 1.13$. The load was a 20 kW induction motor operating at rated power. As can be seen, the left and right side of the reactor share the phase current equally. At one point in the study, the RSS is turned off and only one of the redundant states is used. As can be seen, the reactor currents become unbalanced until the RSS is turned on again. Another method of switching this type of inverter is to alternate back and forth between the redundant states. In this case, the balance will be decent, but there will be some drift from the perfect current sharing case. Therefore, an active RSS control is recommended [7].

3.4.4 DC source current control

For the cascaded H-bridge inverter, it is reasonable to utilize the redundant states to ensure that the power from the dc sources is equalized. This goal can be realized through per-phase RSS. The two-cell topology shown in Figure 3.2-7 with equal dc source voltages can operate with five voltage levels [22]. In this case, the per-phase redundant states can be used to ensure that each cell supplies the same average current [19].

The per-phase redundancy in the cascaded inverter can be further utilized to increase the number of voltage levels. In particular, the two-cell inverter with a binary ratio of the dc source voltages can supply seven voltage levels [49]. Table 3.4-1 shows the specific combinations that make up the voltage levels where the binary ratio has been used by setting $v_{adc1} = 2E$ and $v_{adc2} = E$.

Table 3.4-1. Seven-level H-bridge states.

s_a	s_{aH1}	s_{aH2}	v_{ag1}	v_{ag2}	v_{ag}
0	-1	-1	$-2E$	$-E$	$-3E$
1	-1	0	$-2E$	0	$-2E$
2	-1	1	$-2E$	E	$-E$
	0	-1	0	$-E$	$-E$
3	0	0	0	0	0
4	0	1	0	E	E
	1	-1	$2E$	$-E$	E
5	1	0	$2E$	0	$2E$
6	1	1	$2E$	E	$3E$

The first column in Table 3.4-1 is the overall switching state which matches the general notation produced by multilevel modulation. The next two columns show the individual H-bridge switching states. The output voltages of the H-bridge cells follow their switching states according to Table 3.2-5. The last column shows the overall line-to-ground voltage.

One of the problems with this topology is that the lower-voltage H-bridge cell can experience negative dc currents [49] which can distort the cell voltage if it is fed from an inverter/rectifier supply. The negative dc currents can be eliminated by selection of the redundant states in the following way. For switching states $s_a = 2$ and $s_a = 4$, the redundant cases involving $v_{ag2} = E$ are used when the a-phase current is positive (when the flag is $I_a = 1$). The redundant states involving $v_{ag2} = -E$ are used when $I_a = 0$. Figure 3.4-6 shows the simulated performance. The dc voltage was $E = 110\,\text{V}$ and the modulator commanded a 100 Hz fundamental waveform with a modulation index of $m = 1.13$ and a switching frequency of 10 kHz. The RSS is switched on in the middle of the study. By observing the dc current on the lower-voltage H-bridge cell, it can be seen that the negative current is avoided with RSS.

The intriguing aspect of using RSS to control the current from the dc source is that it considers the transfer function of the load current back to the source which is sometimes overlooked in inverter systems. However, the dc source current can have a significant effect on system performance. In cascaded systems, control of the dc

source current has been used to ensure positive average power from the source [10]. In the three-level diode-clamped topology, the dc source current can be controlled to minimize the capacitor voltage ripple [50].

3.4.5 Switching frequency reduction

Another use for RSS is reduction in the commutation of transistor switches for improvement of drive efficiency. The process involves considering the present transistor switching states and the redundant choices for the next states. The choice can be made based on the state that results in the least number of transistor switches. As with other RSS goals, the state selection can be done off-line and programmed into an RSS table. One example of using RSS for reducing switching frequency is in the single-phase flying capacitor inverter [51] where the capacitor voltage balancing can be included as well. Another application is the series H-bridge with equal dc sources where the redundancy is not needed for capacitor voltage balancing.

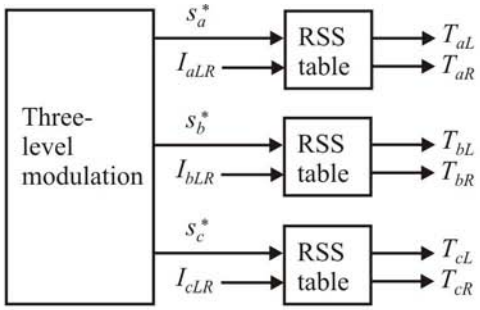

Figure 3.4-4. Parallel phase per-phase RSS tables.

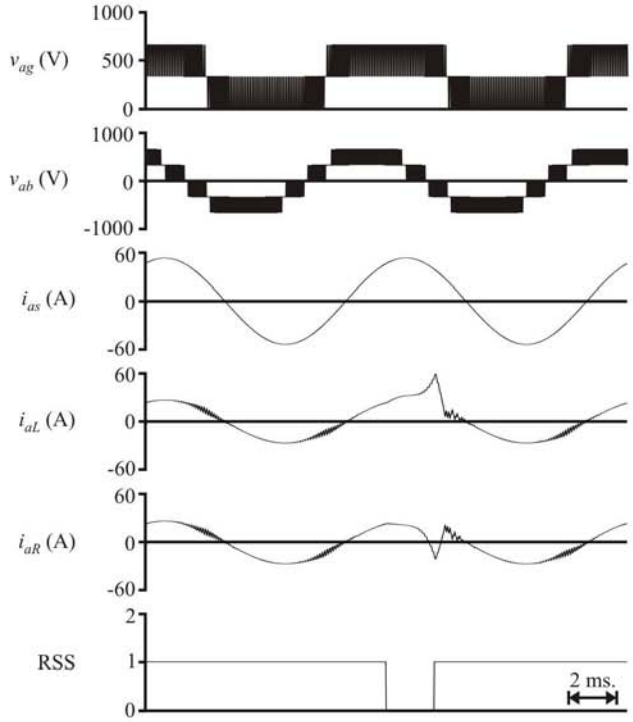

Figure 3.4-5. Three-level parallel inverter performance.

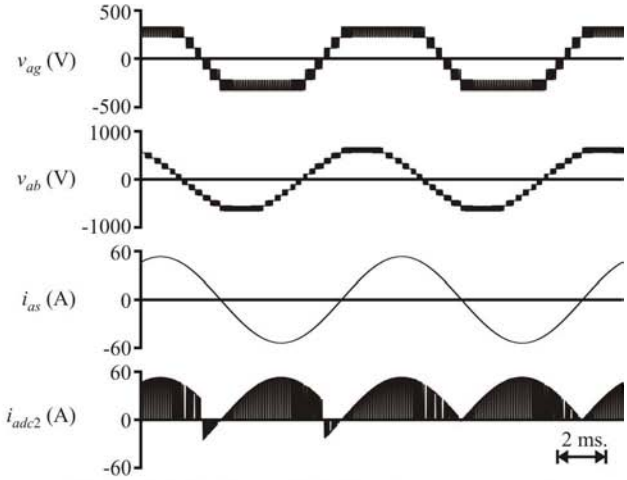

Figure 3.4-6. Series H-bridge inverter waveforms.

3.5 COMBINATIONAL MULTILEVEL TOPOLOGIES

Through parallel and series (cascade) connection of the fundamental topologies, several new topologies can be created. These combinational topologies can have immense advantages over the fundamental topologies. For the cascaded topologies, there is a multiplying effect of the number of levels which leads to exceptional power quality. Furthermore, the combinational topologies typically involve a natural split between a higher-voltage lower-frequency inverter and a lower-voltage higher-frequency inverter. This split matches the physical reality of semiconductor devices.

This section presents three cascaded topologies. The first is a combination of two three-level diode-clamped inverters which are connected through the load. The second is a cascade of five-level and three-level H-bridge cells. The third is a combination of the traditional three-level diode-clamped inverter with five-level H-bridge cells.

3.5.1 Cascaded diode-clamped inverters

Figure 3.5-1 shows the cascade-3/3 inverter. Therein, a three-level diode-clamped inverter supplies a motor load which has a split neutral connection so that the other end of each phase winding can be connected to another three-level inverter. Considering the output voltages, this inverter is similar to the series H-bridge inverter. However, there is an important advantage in that the dc source supplies three phases and cancels the low-frequency single-phase dc currents presented in the series H-bridge system. The suggestion to cascade two three-level inverters in this manner was first made at the European Power Electronics conference in 1993 [8]. In this implementation, both three-level inverter were supplied from isolated dc sources with equal voltages. This effectively operated as a five-level inverter. A few years later, a three-level inverter cascaded with a two-level inverter (cascade-3/2) was introduced [9] as well as the suggestion that one of the sources could be a capacitor supplying only reactive power. The dc voltages had a ratio of two-to-one and the resulting inverter could emulate a four-level inverter. The cascaded diode-clamped inverter was formalized in 1998 for the general case where any number of voltage levels could be used with an arbitrary dc voltage ratio [10]. Furthermore, the ratio to obtain the maximum possible number of voltage levels was introduced. To demonstrate the concept, a cascade-3/2 inverter was created with a four-to-one dc voltage ratio which could operate as a six-level inverter [10]. Recently, there has been much interest in this topic [11,12]. One of the latest advances is the demonstration of the cascade-3/3 inverter operating from just one power source as shown in Figure 3.5-1 [12].

The analysis of the cascade-3/3 inverter is based on the fundamental KVL equations. In this case, a line-to-ground voltage can be defined for each inverter. The phase

voltage equations are similar to (3.1-2) except that the difference of the line-to-ground voltages is used leading to

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{ag} - v_{agx} \\ v_{bg} - v_{bg} \\ v_{cg} - v_{cgx} \end{bmatrix} \tag{3.5-1}$$

Once the ratio between v_{dc} and v_{dcx} has been determined, the phase voltages can be computed in terms of the switching states and the vector diagram can be obtained similar to other multilevel inverters. For the cascade-3/3 inverter, it has been shown that a dc voltage ratio of $v_{dc} = 3v_{dcx}$ yields an effective nine-level inverter and that this is the maxim number of levels that the cascade-3/3 is capable of emulating [10,12]. However, in order to use a capacitor voltage source for the lower-voltage inverter, some voltage levels need to be sacrificed [12]. In particular, if seven voltage levels are used, there is enough redundancy in the system to regulate the floating capacitors and ensure that $v_{dc} = 3v_{dcx}$. The specific details for this inverter control are given in [12] and amount to using the inverter power equations to fill a joint-phase RSS table which works to regulate all capacitor voltages. Figure 3.5-2 shows laboratory measurements of the cascade-3/3 inverter. In this study, the dc source voltage was 600 V and the inverter was driving a 23 kW, 0.86 lagging power factor, R-L load. The top two traces are the line-to-ground voltages of the higher-voltage and lower-voltage inverters. It can be seen that the higher-voltage inverter is switching less often which is desirable from a semiconductor point of view. It is also possible to operate the higher-voltage inverter in a step mode with extremely low switching frequency and still maintain proper inverter operation [12]. The next trace is the *a*-phase load voltage determined by (3.5-1). Due to the high number of levels available, the harmonic distortion for this voltage is $\text{THD}(v_{as}) = 9.00\%$. The next trace is the effective line to line voltage which is calculated as $v_{abs} = v_{as} - v_{bs}$. From this waveform, thirteen distinct voltage levels can be seen as expected from a seven-level inverter. The last trace in Figure 3.5-2 is the *a*-phase current which is essentially a filtered version of the phase voltage.

The cascade-3/3 system of Figure 3.5-1 has several advantages over fundamental multilevel topologies for medium-voltage applications and in particular for Naval ship propulsion [52]. The primary advantage is the high power quality with a relatively low number of semiconductors due the compounding effect of the voltage levels. Another advantage is that only one source is required. This is an advantage for Naval systems where there is typically only one source available and creating extra isolated sources is difficult. Another advantage is that the higher-voltage lower-frequency inverter may be commercial-off-the-shelf meaning that only the lower-voltage inverter needs to be custom built. A final advantage is that the dual nature of the inverter could be used to drive the motor in fault situations. If the primary (higher-voltage) inverter is inoperable, the motor load can be driven by the lower-voltage inverter with system re-configuration.

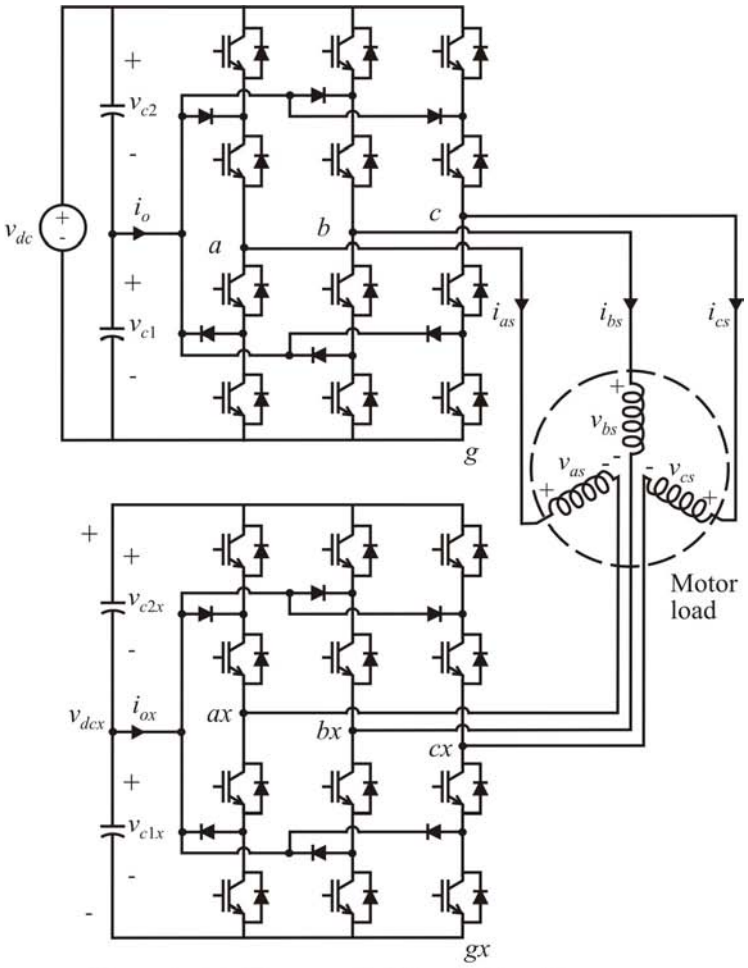

Figure 3.5-1. The cascade-3/3 multi-level inverter.

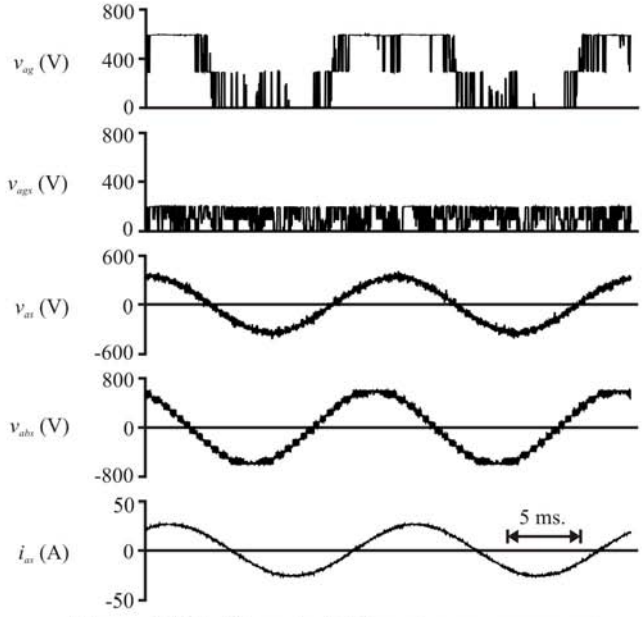

Figure 3.5-2. Cascade-3/3 inverter measurements.

3.5.2 Cascaded multilevel H-bridge inverter

Figure 3.5-3 shows the *a*-phase of the cascade-5/3H inverter where a five-level H-bridge cell is connected in series with a three-level cell. The complete topology involves three phases as depicted in Figure 3.2-7. This is a combinational topology in a couple of senses. First, the five-level cell is a combination of the diode-clamped and H-bridge topologies which was recently patented by GE [21]. Next, the five-level cell is inserted into the series H-bridge inverter in place of a three-level cell. In general any number of cells having any number of levels is possible [53]. The dc voltage ratio can be selected to maximize the number of voltage levels. In this case, setting the ratio to $v_{adc1} = 6v_{adc2}$ yields fifteen levels. However, the maximum case suffers from the disadvantage that negative dc currents in the lower voltage cell will distort the dc voltage if a transformer/rectifier source is used to supply v_{adc2}. One solution to this problem is to use a ratio of $v_{adc1} = 4v_{adc2}$ instead which reduces the number of voltage levels to eleven. Then per-phase RSS can be used to avoid negative dc source currents. Also, per-phase RSS within the five-level cell can be used to ensure that each of the capacitors is charged to one-half of the supply voltage v_{adc1}.

Figure 3.5-4 shows some laboratory measurements of the cascade-5/3H inverter. In this study, the dc voltages were $v_{adc1} = 260\,\mathrm{V}$ and $v_{adc2} = 65\,\mathrm{V}$. The inverter was supplying a 5.2 kW induction motor load at rated power. The top traces are the line-to-line voltage and *a*-phase current which are nearly sinusoidal. The next traces show the *a*-phase capacitor voltages which demonstrate that the per-phase RSS can balance the capacitors.

As with the cascade-3/3 inverter shown in the previous section, it is possible to eliminate one of the dc sources in each phase of the cascade-5/3H inverter by replacing it with a capacitor and sacrificing some voltage levels. In general, any number of cells can be placed in series and only one isolated dc source is needed per phase [54]. For the cascade-5/3H inverter a capacitor source can be used, as shown in Figure 3.5-5, if the number of voltage levels is lowered to nine [54]. Figure 3.5-6 shows laboratory measurements on this inverter. For this study, the dc voltages were $v_{adc1} = 360\,\mathrm{V}$ and $v_{adc2} = 90\,\mathrm{V}$ and the inverter is driving an R-L load. The line-to-ground voltages of the individual cells shows that both cells are switching at nearly the same frequency. This switching was necessary to regulate the capacitor voltages according to per-phase RSS [54]. However, the transistors in the five-level cell will switch at half the frequency of v_{ag1}. The total line-to-ground voltage and phase current appear as expected for a nine-level inverter. The capacitor voltages demonstrate that the per-phase RSS has good control over the capacitor balance.

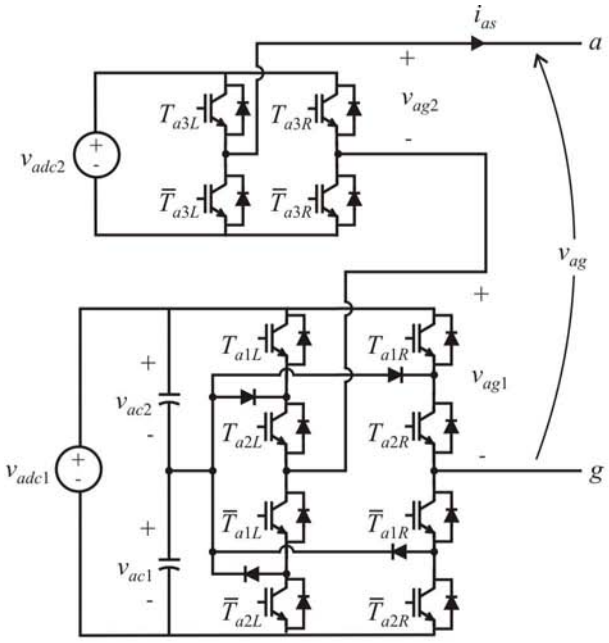

Figure 3.5-3. Cascade-5/3H inverter topology.

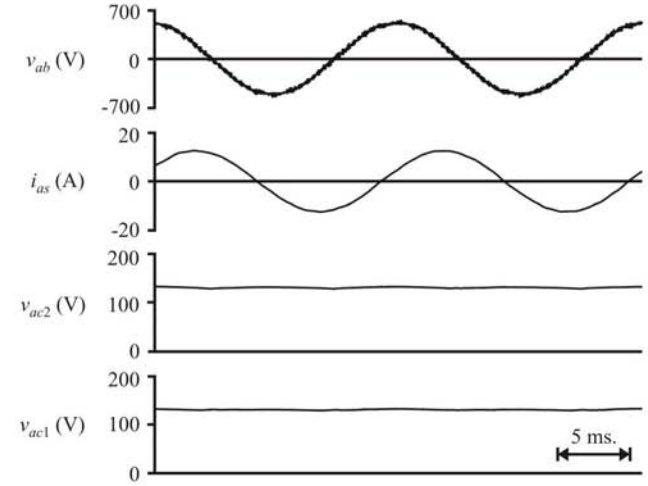

Figure 3.5-4. Cascade-5/3H inverter laboratory measurements.

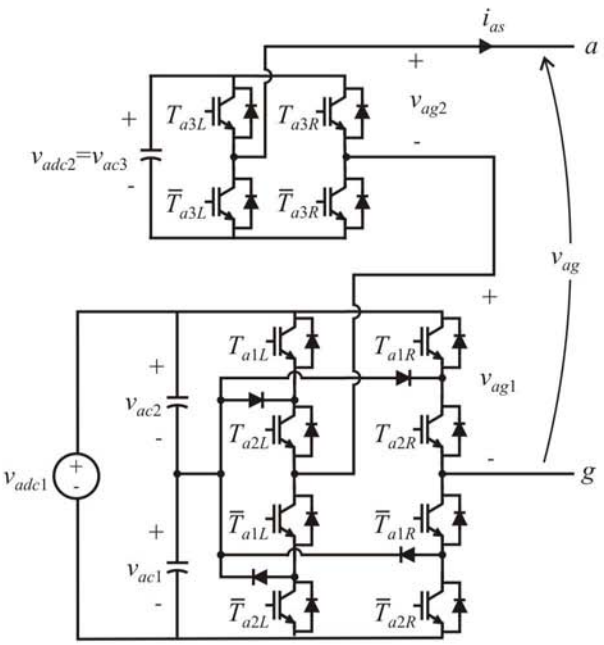

Figure 3.5-5. The cascade-5/3H inverter with capacitor source.

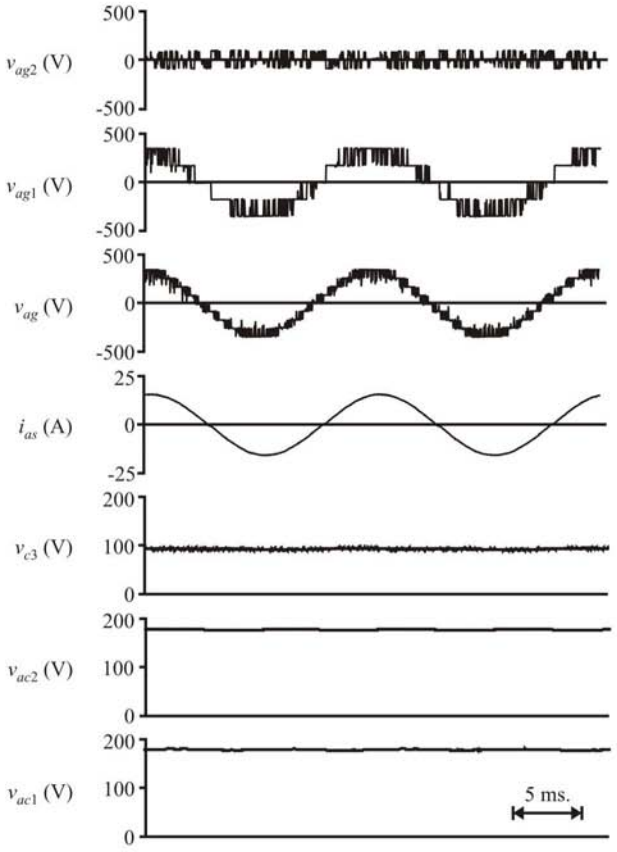

Figure 3.5-6. Cascade-5/3H inverter waveforms.

3.5.3 Cascaded diode-clamped / H-bridge (DCH) inverter

Figure 3.5-7 shows one method of combining the three-level diode-clamped inverter with five-level H-bridge cells (referred to herein as the DCH-3/5 inverter). This topology is similar to that described in a recent patent by ABB [26] with the exception that five-level H-bridge cells are used instead of three-level cells. This inverter can supply fifteen levels if the dc voltage ratio is set to $v_{dc} = 5\left(v_{ac1} + v_{ac2}\right)$. However, some levels must be sacrificed in order to use capacitors instead of isolated dc sources. In particular, if the inverter is operated as an eleven-level inverter, joint-phase RSS can ensure that the floating capacitors will maintain their voltages as well as balance the capacitors on the three-level inverter. Per-phase redundancy within each five-level cell can then ensure that the capacitors of the cell have equal voltages.

Figure 3.5-8 shows the voltage vector plot for the DCH-3/5 inverter which is equivalent to a fifteen-level inverter vector plot. Figure 3.5-9 shows simulated performance of the inverter. In this study, the dc voltage was $v_{dc} = 660\,\mathrm{V}$. The inverter was supplying a 15 kW load with 0.88 lagging power factor. As with the previous cascaded inverter studies, the output voltage contains little harmonics and the capacitor voltages are regulated through RSS.

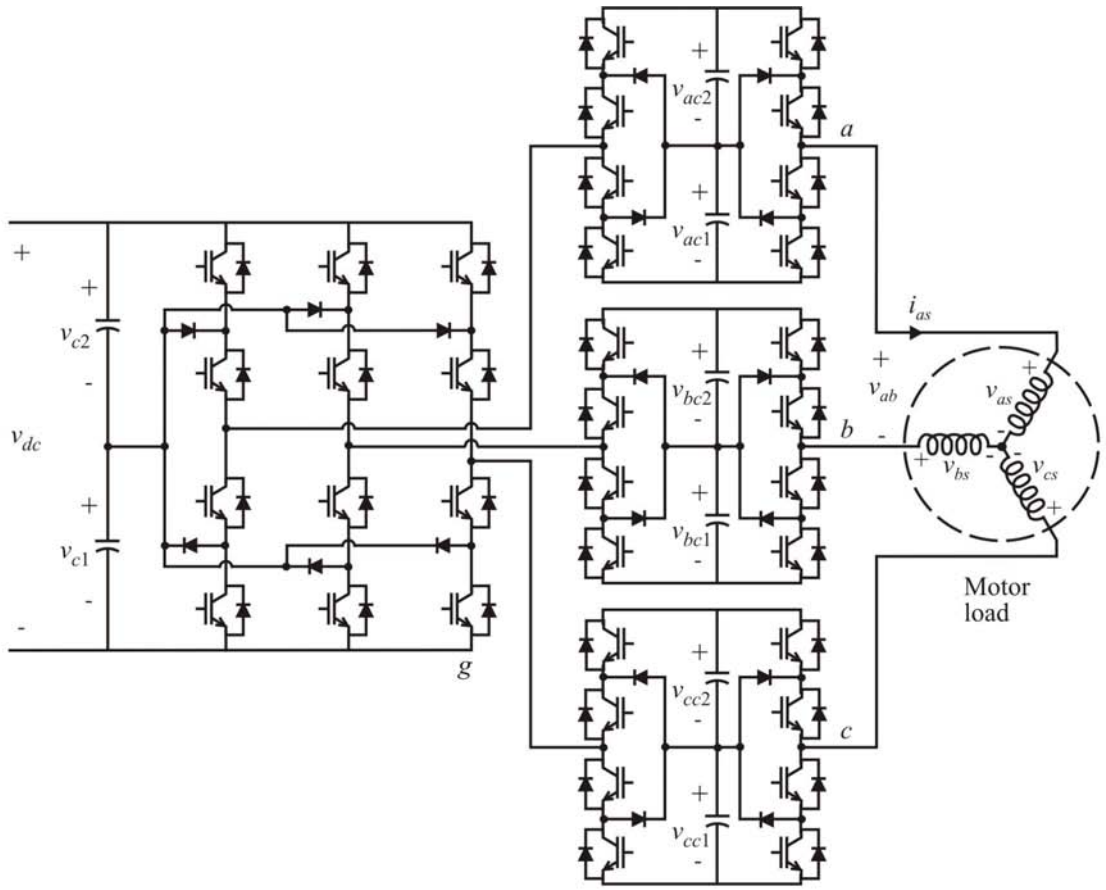

Figure 3.5-7. The three-level diode-clamped / five-level H-bridge DCH inverter.

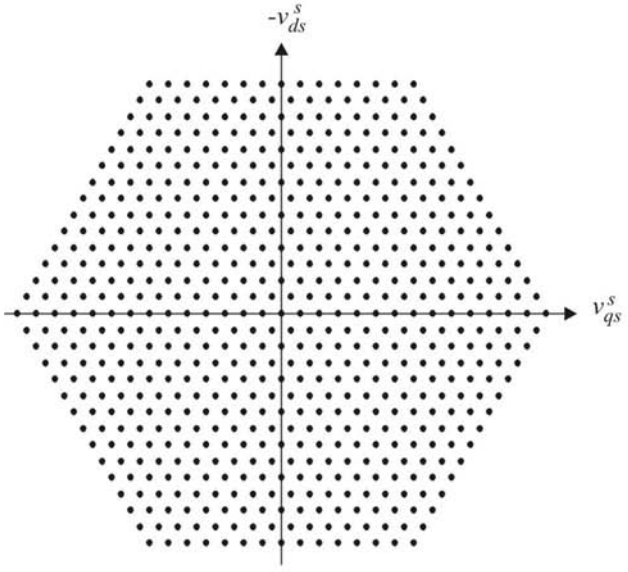

Figure 3.5-8. The DCH-3/5 inverter voltage-vector plot.

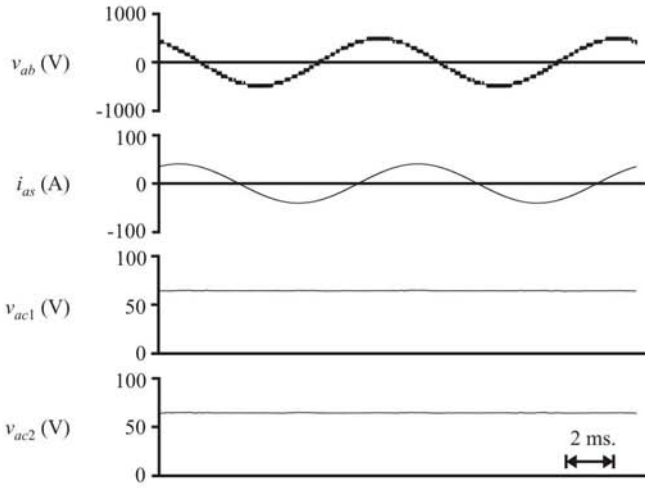

Figure 3.5-9. The DCH-3/5 inverter waveforms.

3.6 ADVANCED STUDY: REDUCED SENSOR AND REDUCED VOLTAGE SOURCE TOPOLOGIES

For many applications, it may be desirable to reduce the number of voltage and current sensors required. Besides a decrease in cost, the reduction of reliance on sensors can be used to increase system reliability in case of sensor failure. In industrial applications, downtime can be reduced (or scheduled) by using a drive system with higher reliability. It may also be desirable to reduce the number of isolated voltage sources required (especially in cascaded multilevel drives). This is particularly true in Navy applications where only one source is available and production of isolated voltage sources increases the volume and weight.

This section introduces methods of observing capacitor voltages in multilevel inverters so that fewer sensors are required. This method is coupled with a method of reducing the number of current sensors and an example is presented using the flying capacitor multilevel inverter. Reduction of isolated voltage sources in cascaded multilevel inverters is then demonstrated on various topologies. The reduced voltage source topologies are then combined with the reduced sensor methods.

3.6.1 Reduced Sensor Topologies

Figure 3.6-1 shows the generalized multilevel converter circuit. It consists of some number of dc voltage sources. Note that any of these sources can be turned into isolated real-power sources by setting the resistance to zero. Alternatively, each source can be specified as a capacitor by setting its dc resistance to infinity. Although most examples contain three phases, there may be any number of phases at the output. Internal to the MLC block are power transistors, power diodes, and electrical connections. Based on a specific topology, a number of transistors are required and their gate inputs are shown at the bottom of the MLC block as $T_1, T_2, T_3, \cdots$. Note that nearly all of the topologies described in previous sections including the diode-clamped, flying capacitor, series H-bridge, and cascaded topologies can be constructed from the generalized circuit by selecting the number of sources and specifying the internal connections. The load may be star connected by an internal connection of the minus terminal of all phases or it may be open (as in the cascaded multilevel inverter). The diode-clamped, structure can be made by internally connecting source capacitors in series. Alternatively, the flying capacitor and series H-bridge structures can be made by internal series connection of power transistor blocks which are connected to external isolated sources.

Figure 3.6-2 outlines the general modeling transfer characteristics of a multilevel power converter. The forward transfer can be defined as the characteristic of

switching the capacitor state variables from the dc side to the ac side based on transistor gate signals. Although this is the focus on most multilevel converter research, it is also interesting to study the reverse transfer which relates the ac side state currents to dc side capacitor currents. The reverse transfer can be utilized to equalize the currents drawn from the dc sources [19,50] or reduce capacitor ripple current [55]. Figure 3.6-2 also depicts derivative and integral relations on the left and right sides. This is to indicate the nature of the relationships and not to depict a pure integral or derivative operation.

In the two-level power converter, the reverse transfer has been used to observe phase currents from the dc current [56]. In this section, this procedure will be applied to the four-level flying capacitor topology shown in Figure 3.6-3. As with the two-level converter, the dc current is directly related to the phase currents and the top transistor signals. For the four-level example, this can be expressed as

$$i_{dc} = T_{a3}\, i_{as} + T_{b3}\, i_{bs} + T_{c3}\, i_{cs} \tag{3.6-1}$$

For the two-level converter, the same expression, involving the top transistors, results. The commonality between the two-level and multilevel flying capacitor inverters comes about because the flying capacitors and their adjacent transistors can be placed inside a network node having the same currents as in the two-level case. For all combinations of top transistor switching states, the dc current is listed in Table 3.6-1. For each switching state (with the exception of the zero-voltage states), the dc current equates to one of the phase currents.

Table 3.6-1. Flying capacitor dc current.

$state_i$	T_{a3}	T_{b3}	T_{c3}	i_{dc}
0	0	0	0	0
1	0	0	1	i_{cs}
2	0	1	0	i_{bs}
3	0	1	1	$i_{bs} + i_{cs} = -i_{as}$
4	1	0	0	i_{as}
5	1	0	1	$i_{as} + i_{cs} = -i_{bs}$
6	1	1	0	$i_{as} + i_{bs} = -i_{cs}$
7	1	1	1	0

Using voltage-source PWM control, there are at most four unique opportunities to observe a phase current within each cycle. As described above, traditional voltage-source PWM creates four unique windows within each DSP switching cycle. This was illustrated in Figure 3.3-4 which shows an example of the switching transitions over one DSP cycle. One method of observing the phase currents is to sample the dc current in the middle of each window. This process can be set-up by computing the sample times in the DSP and communicating this data to a PLD circuit which can

then trigger an analog-to-digital (A/D) converter. The sampled dc current is then combined with the transistor information (T_{a3}, T_{b3}, T_{c3}) to determine which phase current is being sampled. Due to the communication step between the DSP and PLD circuits, the sampled information will not be available for use until the next DSP cycle. However, this delay will not cause significant error in the observed phase currents. Using this new method the existing DSP/PLD controller and one dc current sensor can replace two phase current sensors. For two-level converters, it has been shown that the phase currents can be observed from the dc current sensor with excellent accuracy [56]. In the multilevel flying capacitor converter, it turns out that the currents can not be determined as accurately. The reason for this is the existence of alternate paths for the phase currents through the capacitors. In the two-level converter, the top transistors are switched within every DSP cycle. In the flying capacitor inverter, there are extended periods of time where the top transistors are off (or on) and not switching. During these intervals, the phase current can not be updated and this causes long periods where the observed current is held at a particular value. This effect will be demonstrated in a simulation example below. Although the observed currents are not usable as high-level control signals, they can be effectively used for capacitor voltage balancing where only the current direction is required. As described above, capacitor voltage balancing can be accomplished through redundant state selection (RSS) given the phase current direction and the voltage balance (over-charged or under-charged) for each capacitor. The voltage balance is usually determined using a voltage sensor for each flying capacitor. In the four-level converter, this requires seven (including v_{dc}) voltage sensors. However, it is possible to utilize three voltage sensors measuring the phase-to-ground voltages and then observe the flying capacitor voltages. This is done in a similar way as the phase current observation, but using the forward transfer characteristic. However, at the times when a capacitor is being utilized, it can also being observed and therefore this procedure can determine the flying capacitors with good accuracy.

Table 3.6-2 shows the *a*-phase switching states of the four-level flying capacitor inverter. The dc voltage v_{dc} can be directly observed when the *a*-phase switches to state 7 (as defined in Table 3.6-2). This voltage can also be observed from the *b*- and *c*-phases and so it can be determined accurately. The remaining challenge is to observe the capacitor voltages for each phase. Using the *a*-phase as an example, Table 3.6-2 shows that capacitor voltages v_{ac1} and v_{ac2} are directly determined whenever the *a*-phase switching hits states 4 and 6 respectively. Since the dc voltage can be observed accurately, the capacitor voltages v_{ac1} and v_{ac2} can also be observed whenever the *a*-phase switching hits states 3 and 1 respectively. In states 2 and 5, the observer measures the difference between the two capacitor voltages. For these cases, a memory technique can be used to observe one of the capacitor voltages. This technique relies on saving the most accurate capacitor voltage value. For example, if the modulation and RSS directs the inverter to state 4, the capacitor voltage v_{ac1} is observed. At the same time, the fact that v_{ac1} has been updated (and is more accurate at this point in time than v_{ac2}) is stored in the DSP. If state 2 or 5

is used shortly afterwards, the least accurate voltage (v_{ac2} in this example) can be updated.

Table 3.6-2. Flying capacitor *a*-phase output voltage.

$state_a$	T_{a1}	T_{a2}	T_{a3}	v_{ag}
0	0	0	0	0
1	0	0	1	$v_{dc} - v_{ac2}$
2	0	1	0	$v_{ac2} - v_{ac1}$
3	0	1	1	$v_{dc} - v_{ac1}$
4	1	0	0	v_{ac1}
5	1	0	1	$v_{dc} - v_{ac2} + v_{ac1}$
6	1	1	0	v_{ac2}
7	1	1	1	v_{dc}

The next step to this technique is to determine at which times to observe the capacitor voltages. The voltages can be observed in the middle of each DSP window as with the previous current observation example. Another choice is to update them before and after the state changes. For example, the switching diagram in Figure 3.3-4 shows the DSP cycle divided into two windows for the *a*-phase. The *a*-phase capacitor observation can be performed at times $0.5t_a$ and $0.5(t_a + T_{sw})$. Likewise the *b*- and *c*-phases can be updated according to t_b and t_c.

The above procedure for reducing the number of required sensors was applied to a four-level flying capacitor inverter supplying an R-L load. The initial system uses two phase current sensors, a dc voltage sensor, and six capacitor voltage sensors. The reduced-sensor system uses one dc current sensor and three line-to-ground voltage sensors. The overall sensor requirement has been reduced from nine to four.

The four-level flying capacitor simulation uses the same operating point as the simulations in section 3.1.5. Namely, the load is operating at 1 MVA, 800 kW, 4.16 kV 60 Hz and the dc voltage is 6 kV. The inverter is operating with voltage-source modulation with 5 kHz switching and a modulation index that is 98% of the maximum (defined in equation 3.3-2). A capacitance of $1{,}000\,\mu F$ was used for all capacitors. Figure 3.6-4 shows the *a*-phase variables from the detailed simulation. Therein, the line-to-ground voltage, line-to-line voltage, line-to-neutral voltage, phase current, and flying capacitor voltages are shown. These variables are also labeled in Figure 3.6-3. As can be seen, the ac variables exhibit typical four-level operation; displaying four line-to-ground voltage levels and seven line-to-line voltage levels. The capacitor voltages v_{ac1} and v_{ac2} are regulated to their ideal values of 2 kV and 4 kV respectively by the per-phase RSS balancing control. Figure 3.6-5 shows the same variables for the simulation where the phase current

and capacitor voltage observers are employed. In addition, the observed capacitor voltages (denoted $\tilde{v}_{ac1}$ and $\tilde{v}_{ac2}$) as well as the observed phase current $\tilde{i}_{as}$ are shown. As can be seen, the system operation with four sensors is nearly the same as the case where nine sensors are used. For a quantitative comparison, the capacitor voltage ripple and phase voltage THD are shown in Table 3.6-3.

Table 3.6-3. Four-level FC simulation results.

	Full sensors	Reduced sensors
Δv_{ac1}	2.57 %	4.16 %
Δv_{ac2}	1.22 %	1.65 %
THD(v_{as})	19.37 %	19.38 %

The largest change is seen in the voltage ripple on the lower voltage capacitor which increases by about 1.6 %. The increase in capacitor voltage ripple will transfer to the ac side. However, the increase in phase voltage THD is only 0.01 %. The observed capacitor voltages can be seen to have slightly more ripple than the actual capacitor voltages. One reason for this is the one-sample delay that exists since this particular simulation mimics the action of the DSP and PLD controllers. Another source for this ripple is the relatively low DSP clock frequency of 5 kHz. In a lower power system, this frequency can be increased which will lead to an even more accurate observation of the capacitor voltages. As mentioned earlier, the observed phase current will not be accurate for extended periods of time when the top transistors are not switching. This is seen by the flat portions (held values) in the observed current waveform. The asymmetry in this waveform comes about from the RSS capacitor voltage balancing which is utilizing different transistor combinations depending on the state of the capacitor voltage balance. In a two-level converter, the top transistors switch at the DSP clock period and the resulting observed current is much more accurate [56]. Since this signal was used for capacitor voltage balancing, only the polarity was significant. Therefore, the capacitor voltage balance based on the observed current worked well. It should also be pointed out that the RSS method was used as an example in this paper, but the reduced sensor methods presented in this section will work with other flying capacitor controls presented in the literature.

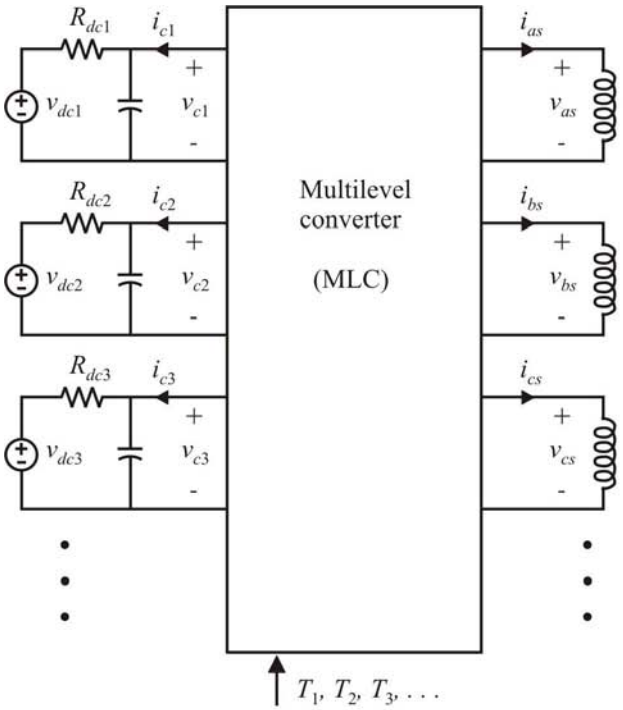

Figure 3.6-1. The general multilevel converter structure.

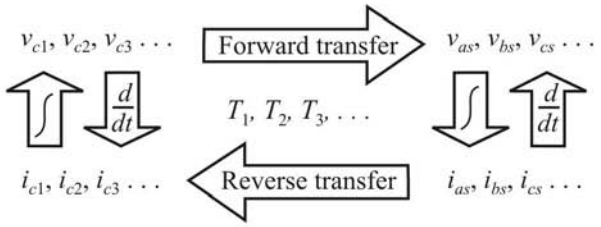

Figure 3.6-2. Multilevel converter transfer characteristics.

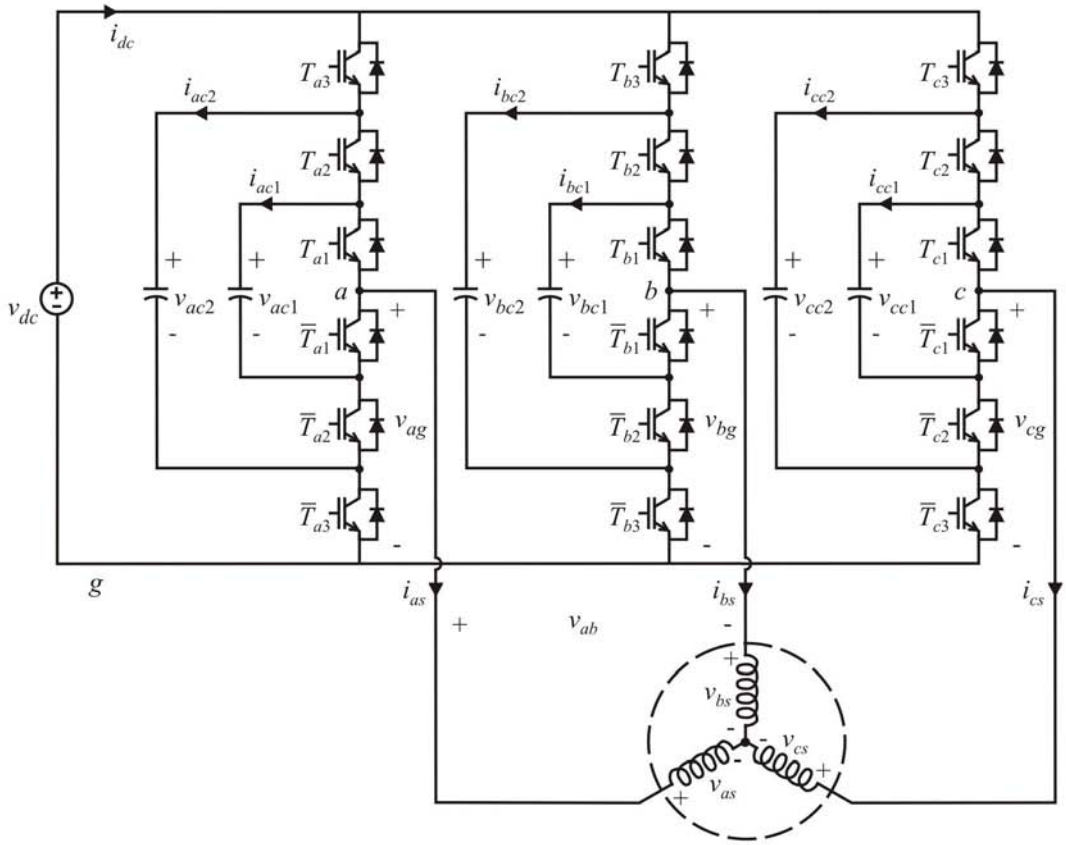

Figure 3.6-3. Four-level flying capacitor inverter topology.

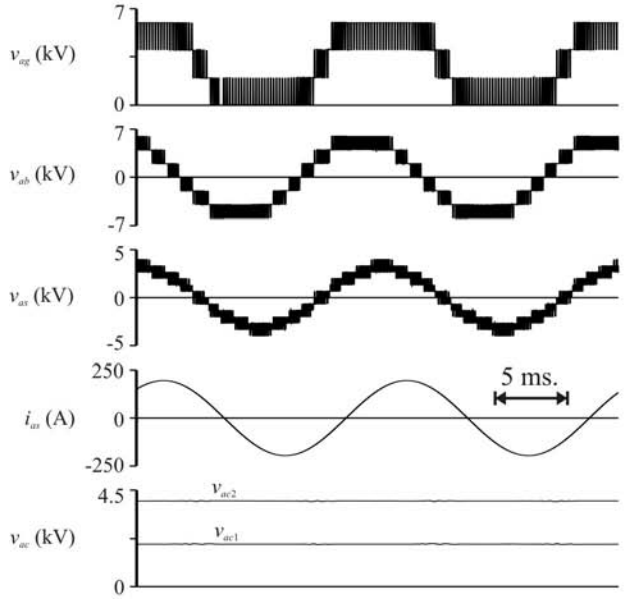

Figure 3.6-4. Flying capacitor simulation (full sensors).

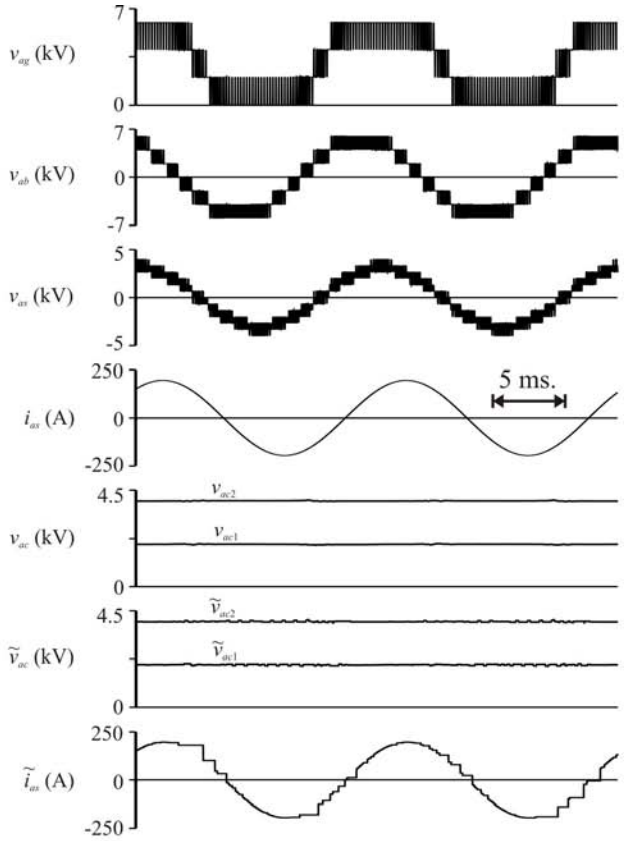

Figure 3.6-5. Flying capacitor simulation (reduced sensors).

3.6.2 Reduced Voltage Source Topologies

In this section, several multilevel inverter examples will be considered in which the requirement of supplying isolated dc voltage sources is reduced. The first example is the cascade-5/3H inverter shown in Figure 3.6-6. This topology is the same as the a previous example introduced in section 3.5-2. However, the performance is extended by setting the dc voltage ratio so as to maximize the number of ac voltage levels. In particular, setting the ratio to $v_{adc1} = 6v_{adc2}$ yields fifteen levels. This can be seen by considering the voltage vector plot shown in Figure 3.6-7. The vectors indicated by large dots are the voltage vectors of the five-level cells around which a three-level pattern forms indicated by the small dots. In section 3.5-2, per-phase RSS was used to reduce the performance to nine-level operation. In this example, the base performance is fifteen-level, but it will be reduced to thirteen-level so that the top H-bridge cells can be supplied from capacitor sources as shown in Figure 3.6-6. The principle is identical to the RSS method of the cascade-3/3 example in section 3.5-1 above [12]. Essentially, if the commanded voltage is kept within the limits of the real dc voltage source which supplies the five-level cells, there will always be redundant states available to regulate the capacitor voltages of the three-level cells. In Figure 3.6-7, this limit is indicated by the dashed hexagon. Although it is beyond the scope of this monograph, it is possible to extend the performance to fourteen-level and still maintain balance of the capacitor voltages [57]. Figure 3.6-8 shows the simulated inverter performance where all six cells are supplied from real power sources. The operating conditions are the same as previous examples. In particular, the load is operating at 1 MVA, 800 kW, 4.16 kV, and 60 Hz. The dc voltage on the five-level cells was set to the full voltage $v_{adc1} = v_{bdc1} = v_{cdc1} = 3\,\text{kV}$. Using this voltage ratio, the three-level cells are supplied by $v_{adc2} = v_{bdc2} = v_{cdc2} = 0.5\,\text{kV}$. This yields an overall real dc voltage which is higher than the previous examples by 1 kV. However, this was selected to match the case when the three-level cells are supplied from capacitors and the real-power dc source voltage will total 6 kV (plus and minus 3 kV). The increase in dc voltage is compensated by a decrease in the modulation index. One way of calculating the new modulation index is to ratio it by the desired dc voltage (6 kV) over the total dc voltage (7 kV). To match the previous examples, the modulation index is set to 98% of the maximum. However, in this case it is (6/7)*98% which is 84%. This modulation index is used in a fifteen-level modulator resulting in thirteen-level performance and the appropriate voltage magnitude output. In Figure 3.6-8, the line-to-ground voltage v_{ag}, the line-to-line voltage v_{ab}, the line-to-neutral voltage v_{as}, phase current i_{as}, and dc source voltage v_{adc2} are shown. The line-to-ground voltage shows asymmetry because of the RSS control. For each switching state, the RSS control reduces the switching states to its lowest possible levels (by reducing the switching states of all phases at the same time) and then incrementing the switching states to find the best one in terms of capacitor voltage balancing. However, this topology is supplied from real-power sources and so the result is a

reduction in the voltage level in all phases. Since this is a common-mode line-to-ground change (the same in all phases), it does not affect the line-to-line and line-to-neutral voltages of the load as can be seen in Figure 3.6-8. Another way to state this is that the harmonics of v_{ag} contain significant terms which are a multiple of three times the fundamental and therefore cancel according to (3.1-2) and (3.1-3). Figure 3.6-9 shows the simulation results for the case where the three-level cells are supplied by capacitor sources with a value of $1{,}000\,\mu\text{F}$ per phase. In this case, the reduction in modulation index and RSS is needed to effectively regulate the capacitor voltage to 1 kV. Although the voltage ripple is visible, it is small compared to the effective dc voltage of 6 kV and therefore does not distort the load voltages.

The previous example demonstrated a reduction of real-power sources from six to three. This benefit is even more pronounced when the number of cells is increased. Figure 3.6-10 shows the cascade-3/3/3H inverter. Although it is made from three-level cells, the multiplying effect of three cells yields a potential twenty-seven level performance if the dc voltage ratio is set according to $v_{adc1} = 3v_{adc2} = 9v_{adc3}$.The resulting voltage vector plot is shown in Figure 3.6-11. Therein, twenty-seven level capability is seen. As with the previous example, the bold voltage vectors are from the highest-voltage cells. In this case, these vectors form a three-level pattern. Although the detail is not depicted, the vectors indicated by smaller dots come from a three-level pattern around each of the large dots followed by another three-level pattern around these vectors. A dashed hexagon indicates the boundaries of operation based on the value of the real-power dc source. Operation within this hexagon allows regulation of the capacitor voltages of the upper two cells. Figure 3.6-12 shows the simulated waveforms of the cascade-3/3/3H inverter where all nine H-bridge cells are supplied by real-power sources. The simulation conditions are the same as with previous examples. In this example, the dc voltages are set to $v_{adc1} = v_{bdc1} = v_{cdc1} = 3\,\text{kV}$, $v_{adc2} = v_{bdc2} = v_{cdc2} = 1\,\text{kV}$, and $v_{adc3} = v_{bdc3} = v_{cdc3} = 0.5\,\text{kV}$. As with the previous example, the total voltage will be larger than required in the case where all nine isolated sources are used. In order to have the rated load voltage, a twenty-seven level modulator was used with a modulation index of 67.8% of its maximum value. In Figure 3.6-12, the line-to-ground voltage v_{ag}, line-to-line voltage v_{ab}, line-to-neutral voltage v_{as}, phase current i_{as}, and *a*-phase dc source voltages v_{adc2} and v_{adc3} are shown. One of the interesting properties for this inverter is the exceptional power quality. In this case, the line-to-neutral voltage is nearly sinusoidal with a THD of 3.51%. Figure 3.6-13 shows the simulation of the same system with reduced voltage sources. The line-to-ground voltage shows an increase in switching frequency due to RSS balancing of the capacitor sources. This yields a stable voltage for the capacitors which is seen in Figure 3.6-13. The capacitor values were $9{,}300\,\mu\text{F}$ leading to low voltage ripple of 0.87% for v_{adc2} and 2.03% for v_{adc3}. The resulting line-to-neutral voltage THD is 3.51% (the same as the simulation with nine isolated dc sources).

The number of voltage sources can be further reduced in the twenty-seven level topology by using a standard three-level inverter in place of three H-bridge cells. This combinational topology will be referred to as the DCH-3/3/3 inverter and provides a simple method of cascading multilevel inverters [26,58]. If the H-bridge cells can be supplied from capacitor sources, only one real-power source is required. The vector plot and modulation conditions are very similar to the cascade-3/3/3H example considered above. The dc voltages are also the same with $v_{dc} = 6\,\text{kV}$. Figures 3.6-15 and 3.6-16 show the simulation results with a full set of isolated real-power voltage sources and reduced sources respectively. The line-to-neutral voltage THD is 3.51% in both cases. In the reduced source case, the capacitor voltage ripple is 1.05% for v_{adc2} and 2.16% for v_{adc3}. The capacitors have values of $9{,}300\,\mu\text{F}$. In this example, the number of isolated sources required was reduced from seven to one.

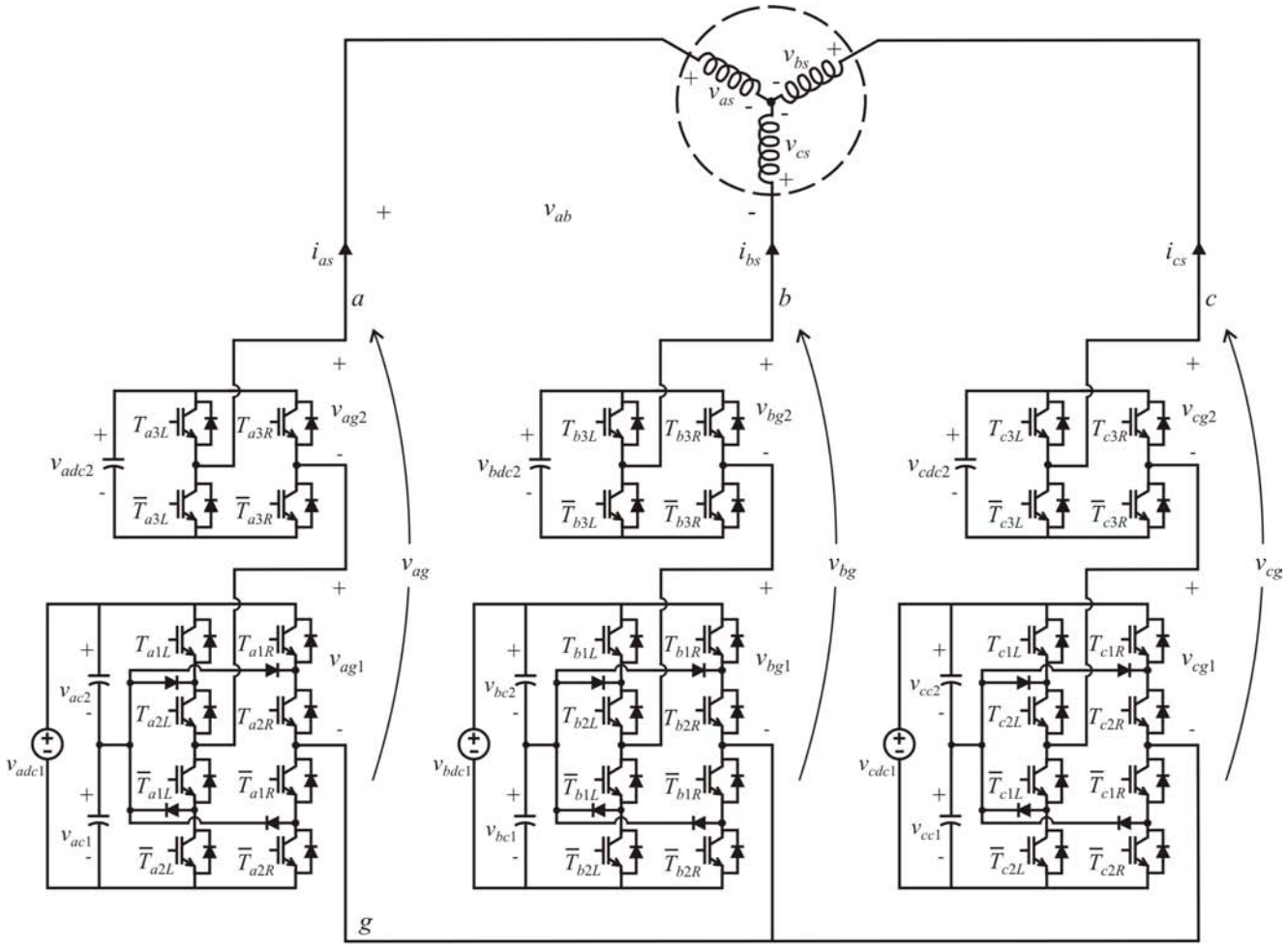

Figure 3.6-6. The cascade-5/3H inverter topology.

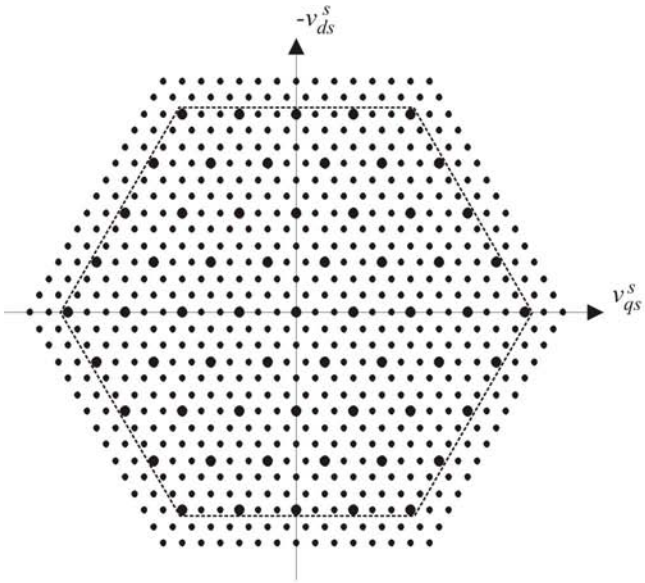

Figure 3.6-7. Vector plot of the cascade-5/3H inverter.

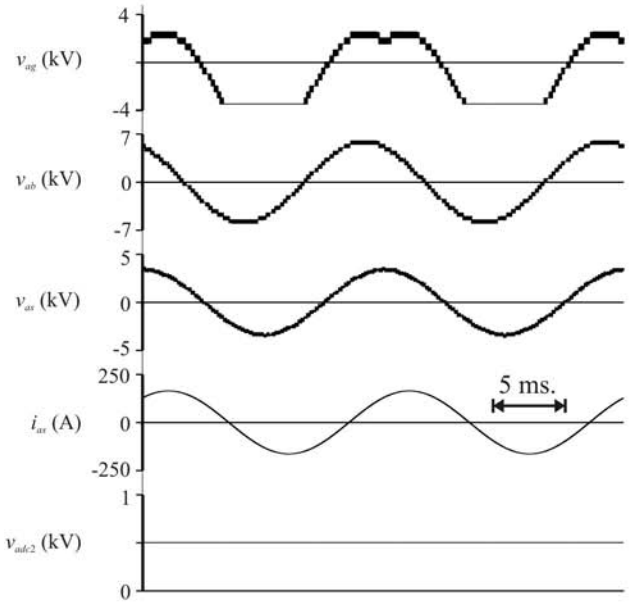

Figure 3.6-8. Cascade-5/3H inverter simulation (6 sources).

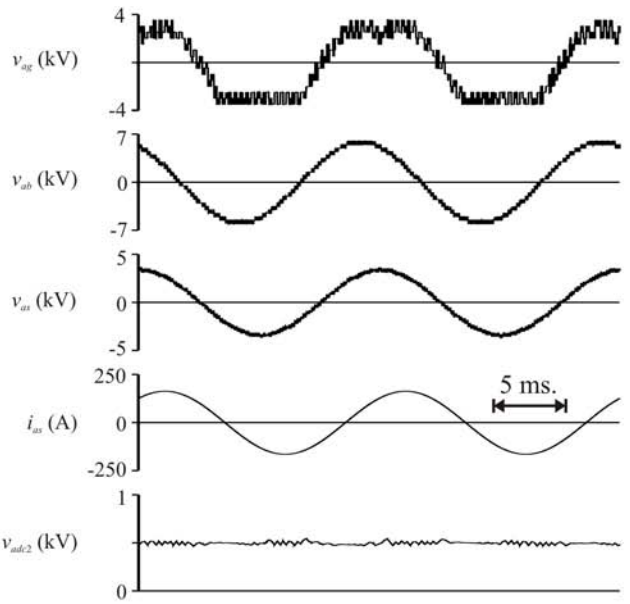

Figure 3.6-9. Cascade-5/3H inverter simulation (3 sources).

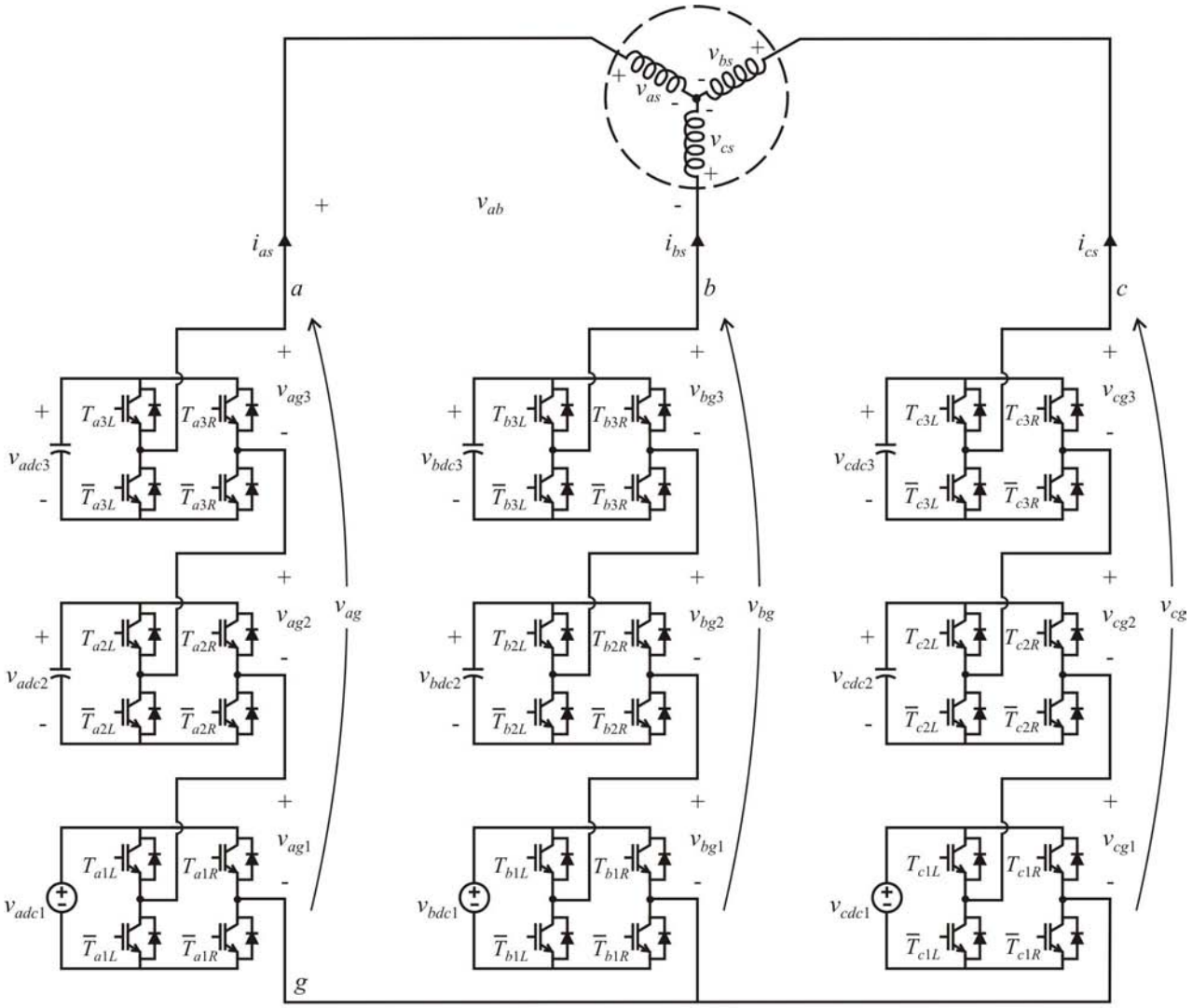

Figure 3.6-10. The cascade-3/3/3H topology

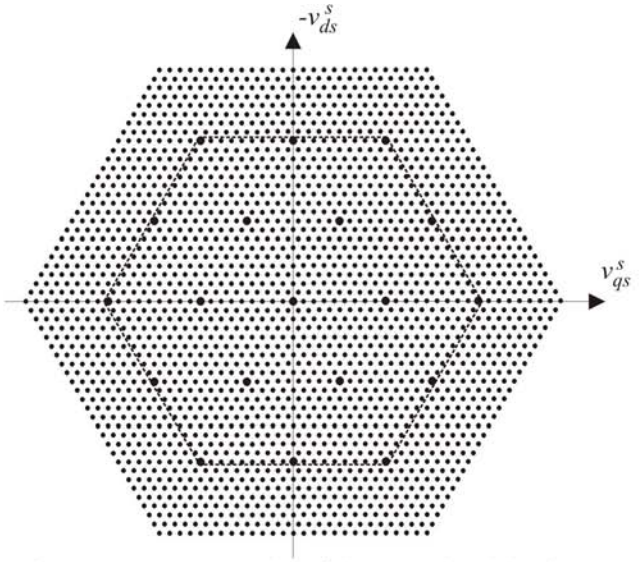

Figure 3.6-11. Vector plot of the cascade-3/3/3H inverter

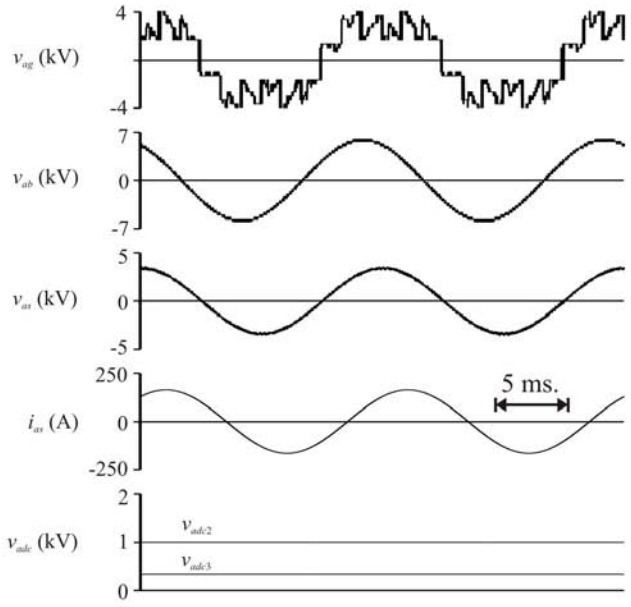

Figure 3.6-12. Cascade-3/3/3H inverter simulation (9 sources).

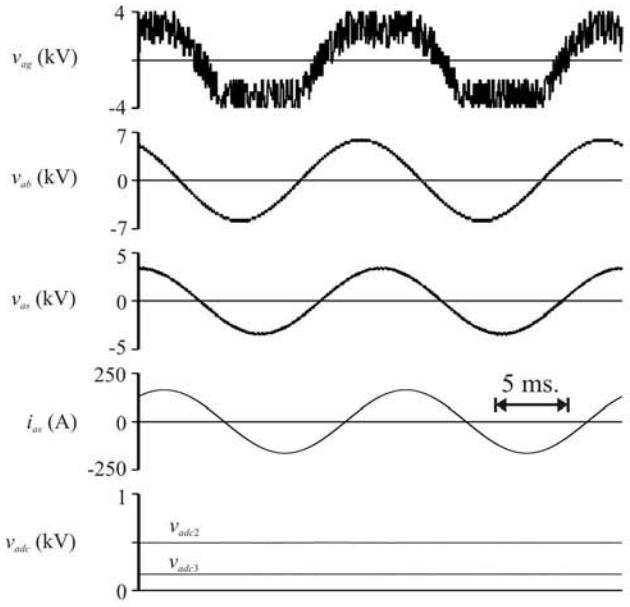

Figure 3.6-13. Cascade-3/3/3H inverter simulation (3 sources).

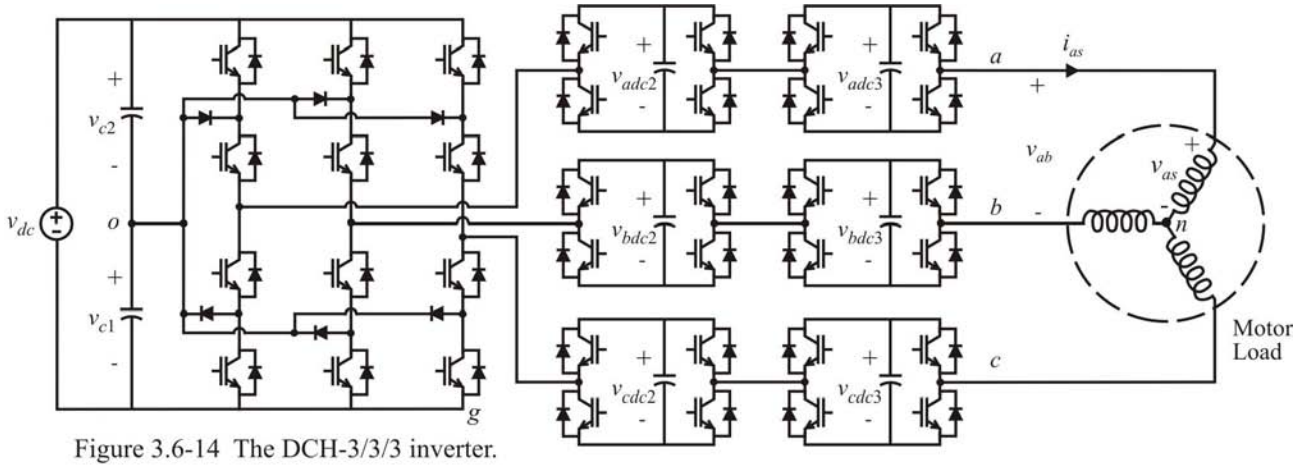

Figure 3.6-14 The DCH-3/3/3 inverter.

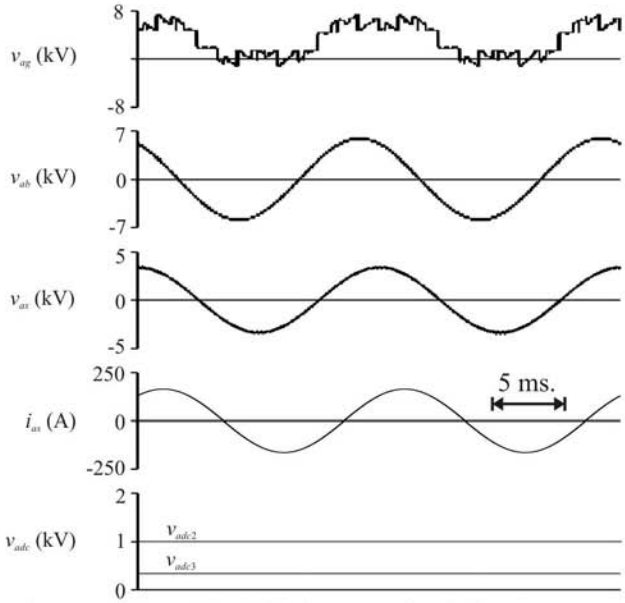

Figure 3.6-15. DCH-3/3/3 inverter simulation (7 sources).

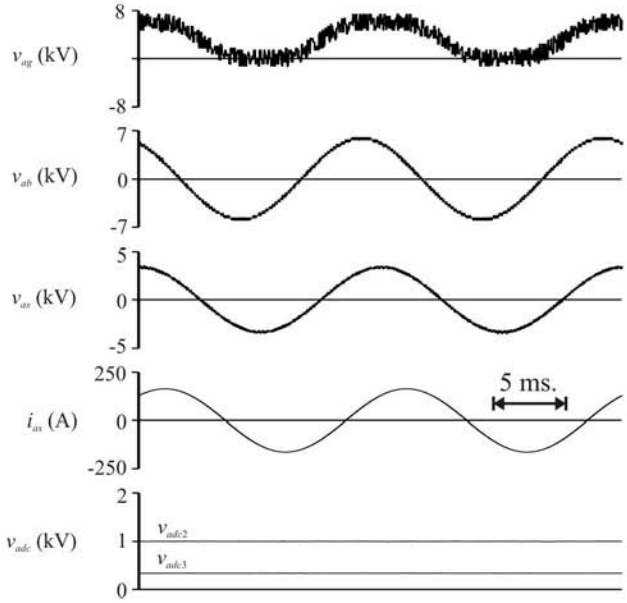

Figure 3.6-16. DCH-3/3/3 inverter simulation (1 source).

3.6.3 Reduced Sensor and Voltage Source Topologies

The DCH-3/3/3 topology shown in Figure 3.6-14 is an effective multilevel inverter having a straightforward construction and exceptional power quality. By regulating the capacitor voltages through RSS control, only one real-power dc voltage source is required. This is significant in applications such as Naval ship propulsion where one source is available and obtaining additional isolated dc sources adversely affects the volume and weight. For this mode of operation, the RSS control will require knowledge of the floating capacitor voltages v_{adc2}, v_{adc3}, v_{bdc2}, v_{bdc3}, v_{cdc2}, and v_{cdc3} as well as v_{c1} and v_{c2}. These eight sensors can be replaced by three line-to-midpoint sensors and an the capacitor voltage observation method introduced in section 3.6.1. The line-to-midpoint voltages are labeled v_{ao}, v_{bo}, and v_{co} and are the voltages from the phase a, b, and c to the dc midpoint o respectively. Table3.6-4 shows the forward transfer of the line-to-midpoint voltage from the capacitor voltages for the *a*-phase. Therein, the switching state s_a is a global state of all cascaded inverters and represents the twenty-seven unique voltage levels. Switching states s_{a1}, s_{a2}, and s_{a3} are the individual switching states for the diode-clamped phase leg and H-bridge inverter cells. As defined previously, a switching state of 0 represents the lowest possible voltage and the highest voltage is represented by the number of levels minus 1. By considering the voltage output v_{ao} in Table 3.6-4 and the ideal values of the voltages $v_{c1} = v_{c2} = 3\,\text{kV}$, $v_{adc2} = v_{bdc2} = v_{cdc2} = 1\,\text{kV}$, and $v_{adc3} = v_{bdc3} = v_{cdc3} = 0.5\,\text{kV}$ twenty-seven even voltage levels can be verified.

Table 3.6-4. DCH-3/3/3 *a*-phase switching states and sensor voltage.

s_a	s_{a1}	s_{a2}	s_{a3}	v_{ao}
0	0	0	0	$-v_{c1}-v_{adc2}-v_{adc3}$
1	0	0	1	$-v_{c1}-v_{adc2}$
2	0	0	2	$-v_{c1}-v_{adc2}+v_{adc3}$
3	0	1	0	$-v_{c1}-v_{adc3}$
4	0	1	1	$-v_{c1}$
5	0	1	2	$-v_{c1}+v_{adc3}$
6	0	2	0	$-v_{c1}+v_{adc2}-v_{adc3}$
7	0	2	1	$-v_{c1}+v_{adc2}$
8	0	2	2	$-v_{c1}+v_{adc2}+v_{adc3}$
9	1	0	0	$-v_{adc2}-v_{adc3}$
10	1	0	1	$-v_{adc2}$
11	1	0	2	$-v_{adc2}+v_{adc3}$
12	1	1	0	$-v_{adc3}$
13	1	1	1	0
14	1	1	2	v_{adc3}
15	1	2	0	$v_{adc2}-v_{adc3}$
16	1	2	1	v_{adc2}
17	1	2	2	$v_{adc2}+v_{adc3}$
18	2	0	0	$v_{c2}-v_{adc2}-v_{adc3}$
19	2	0	1	$v_{c2}-v_{adc2}$
20	2	0	2	$v_{c2}-v_{adc2}+v_{adc3}$
21	2	1	0	$v_{c2}-v_{adc3}$
22	2	1	1	v_{c2}
23	2	1	2	$v_{c2}+v_{adc3}$
24	2	2	0	$v_{c2}+v_{adc2}-v_{adc3}$
25	2	2	1	$v_{c2}+v_{adc2}$
26	2	2	2	$v_{c2}+v_{adc2}+v_{adc3}$

As described in section 3.6-1, the capacitor voltage observation algorithm can perform a sample in the middle of each of the four windows formed within a DSP switching cycle (illustrated in Figure 3.3-4). The algorithm works in the following way. Any state in which one H-bridge cell outputs zero voltage allows for observation of the other H-bridge cell (assuming that its output is not commanded to zero). For example, in states where $s_{a2}=1$ and $s_{a3}\neq 1$ the voltage v_{adc3} can be estimated using

$$\tilde{v}_{adc3}=\frac{v_{ao}-v_{a1o}}{s_{a3}-1} \tag{3.6-2}$$

where v_{a1o} is the *a*-phase line-to-midpoint voltage of the diode-clamped inverter which can be determined by

$$v_{a1o}=\begin{cases}-\tilde{v}_{c1} & s_{a1}=0\\ 0 & s_{a1}=1\\ \tilde{v}_{c2} & s_{a1}=2\end{cases} \tag{3.6-3}$$

In (3.6-2) and (3.6-3) the ~ symbol is used to represent observed voltages since the DSP can only read v_{ao}. According to the conditions of observation, (3.6-2) will be implemented whenever s_a has values of 3, 5, 12, 14, 21 and 23 as shown in Table 3.6-4. For states where $s_{a2}\neq 1$ and $s_{a3}=1$ the voltage v_{adc2} can be estimated using

$$\tilde{v}_{adc2}=\frac{v_{ao}-v_{a1o}}{s_{a2}-1} \tag{3.6-4}$$

This includes states where s_a has values of 1, 7, 10, 16, 19, and 25. The observation of v_{c1} and v_{c2} takes place in the states where $s_{a2}=1$ and $s_{a3}=1$ which includes states where s_a has values of 4 and 22. At these states, the capacitor voltages can be observed using

$$\begin{aligned}\tilde{v}_{c1}&=-v_{ao} \quad \text{if } s_{a1}=0\\ \tilde{v}_{c2}&=v_{ao} \quad \text{if } s_{a1}=2\end{aligned} \tag{3.6-5}$$

Figure 3.6-17 shows the simulated DCH-3/3/3 performance for the case where one source is utilized and three voltage sensors are used to observe all eight capacitor voltages. As can be seen, the performance is similar to the full sensor cases shown in Figures 3.6-15 and 3.6-16. In addition, the observed capacitor voltages for the *a*-phase are shown. Due to the fact that the voltages are being observed and then regulated through RSS, and the simulation includes details of the DSP switching

times, the capacitor voltage ripples are higher than in the full sensor case. In particular, the ripple is 9.29% for v_{adc2} and 18.4% for v_{adc3}. However, since the average voltage is low relative to the total dc voltage, the effect on the output voltage is not seen. The line-to-neutral voltage THD has increased from 3.51% in the previous example to only 3.55% in the reduced sensor example. In this case, the DCH-3/3/3 inverter is operating with one isolated dc source and three voltage sensors instead of eight.

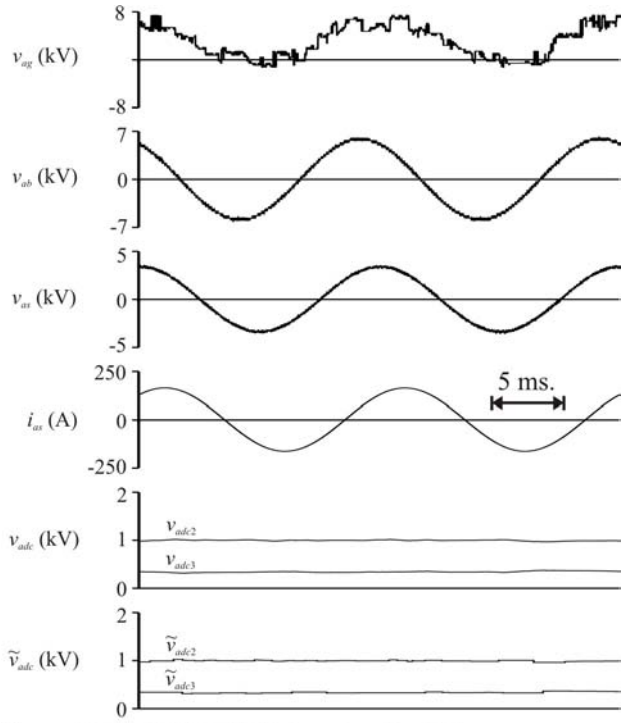

Figure 3.6-17. DCH-3/3/3 inverter simulation (1 source and reduced sensors).

3.7 CONCLUDING REMAKS

This monograph has been an attempt to summarize the present state of multilevel power conversion. Although numerous topologies and modulation methods were discussed, several more can be found in the references and in the literature. An additional goal of this monograph was to introduce concepts related to reducing the number of isolated voltage sources and sensors. This can be important in the high power quality cascaded multilevel inverters which require several voltage sources and knowledge of the dc voltage levels. Applications of the cascaded multilevel inverter include Naval ship propulsion which necessitates high power quality.

The general concept of multilevel power conversion was introduced more than twenty years ago. However, most of the development in this area has occurred over the past five years. Furthermore, each year seems to bring even more publications than the previous. Besides the mainstream power electronics conferences and journals, multilevel power conversion is also showing up in power systems and electronics societies. Despite the rapid growth of this area in recent years and the increasing number of innovations introduced each year, there is still much more that can be done. The author has contributed to this field over the past ten years and encourages other researchers to expand this work in the context of other, closely related, research areas eluded to herein.

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