

Extended Operation of Flying Capacitor Multilevel Inverters

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Abstract—Recent research in flying capacitor multilevel inverters (FCMIs) has shown that the number of voltage levels can be extended by changing the ratio of the capacitor voltages. For the three-cell FCMI, four levels of operation are expected if the traditional ratio of the capacitor voltages is 1:2:3. However, by altering the ratio, the inverter can operate as a five-, six-, seven-, or eight-level inverter. According to previous research, the eight-level case is referred to as maximally distended (or full binary combination schema) since it utilizes all possible transistor switching states. However, this case does not have enough per-phase redundancy to ensure capacitor voltage balancing under all modes of operation. In this paper, redundancy involving all phases is used along with per-phase redundancy to improve capacitor voltage balancing. It is shown that the four- and five-level cases are suitable for motor drive operation and can maintain capacitor voltage balance under a wide range of power factors and modulation indices. The six-, seven-, and eight-level cases are suitable for reactive power compensation in applications such as static var compensation. Simulation and laboratory measurements results verify the proposed joint-phase redundancy control.

Keywords- Multi-level, inverter, rectifier, converter, flying capacitor, voltage balancing.

I. INTRODUCTION

In recent years there has been considerable development in multilevel power conversion, especially in the area of medium-voltage drives. The flying capacitor multilevel inverter (FCMI) topology [1-10] is relatively new compared to the diode-clamped [11-13] and series H-bridge [14,15] inverters. Although the FCMI is not as common, it has some distinct advantages over the diode-clamped topology including the absence of clamping diodes and the ability to regulate the flying capacitor voltages through redundant state selection even if the number of voltage levels is greater than three [1-10]. Unlike the series H-bridge inverter, isolated voltage sources are not required. Considering these advantages, the FCMI is finding many practical applications in industry [2].

The reason that capacitor voltage balancing is not an issue in the FCMI is that there are several conduction paths within each phase that can produce the same voltage levels. This per-phase redundancy can be used to choose the path with the best balancing characteristics at any point in time. It is possible to change the ratio of capacitor voltages and sacrifice this redundancy in order to improve the power quality by increasing the number of voltage levels [3]. However, some of the

redundant states are then not available for capacitor balancing. Therefore, a tradeoff between power quality and capacitor balancing can be established. In this paper, a three-cell flying capacitor inverter is used to exemplify this tradeoff. The typical four-level performance is extended to five-, six-, seven-, and eight-level. The loss in capacitor voltage balancing control is compensated by using joint redundancy involving all phases (in effect adjusting the common-mode line-to-ground voltage). It is shown that five-level operation can be achieved for motor drive applications, while six-, seven- and eight-level operation are possible for applications involving reactive power compensation.

II. THE FLYING CAPACITOR INVERTER

Figure 1 shows one phase of the three-cell flying-capacitor inverter topology. For this inverter, each capacitor is charged to a different voltage level and by changing the transistor switching states, the capacitors and dc source are connected in different ways and produce various line-to-ground output voltages. For the analysis presented herein, the line-to-ground voltage and capacitor currents are of interest. From the topology KVL and KCL equations, these quantities can be expressed as

$$v_{ag} = (T_{a3})v_{dc} + (T_{a2} - T_{a3})v_{c2a} + (T_{a1} - T_{a2})v_{c1a}, \quad (1)$$

$$i_{c1a} = (T_{a2} - T_{a1})i_{as}, \quad (2)$$

$$i_{c2a} = (T_{a3} - T_{a2})i_{as}. \quad (3)$$

Based on these fundamental equations, the line-to-ground voltage and capacitor currents can be determined for all combinations of transistor signals as shown in Table I.

As with other inverter topologies, the three-phase implementation involves three branches of the structure shown in Figure 1 connected in parallel on the dc side and connected to a wye-configured load on the ac side. Since the load neutral may not be accessible, the line-to-line voltages may be of interest and can be expressed in terms of the line-to-ground voltage by [3]

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix}. \quad (4)$$

TABLE I. THREE-CELL FCMI OUTPUT VOLTAGES

T_{a1}	T_{a2}	T_{a3}	v_{ag}	i_{c1a}	i_{c2a}
0	0	0	0	0	0
0	0	1	$v_{dc} - v_{c2a}$	0	i_{as}
0	1	0	$v_{c2a} - v_{c1a}$	i_{as}	$-i_{as}$
0	1	1	$v_{dc} - v_{c1a}$	i_{as}	0
1	0	0	v_{c1a}	$-i_{as}$	0
1	0	1	$v_{dc} - v_{c2a} + v_{c1a}$	$-i_{as}$	i_{as}
1	1	0	v_{c2a}	0	$-i_{as}$
1	1	1	v_{dc}	0	0

The load line-to-neutral voltage can also be determined directly from the line-to-ground voltages using [3]

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix}. \quad (5)$$

Unlike the diode-clamped topology, there are no restrictions on the transistor states and all eight combinations of transistor signals are valid. Table II shows the a -phase line-to-ground voltage v_{ag} for all switching states considering different voltage ratios. The voltage ratios in Table II are listed as $(v_{c1a}:v_{c2a}:v_{dc})$. In fact, there are several ratios that can lead to four-, five-, six-, seven-level or eight-level operation. However, just one ratio is shown for each case in the interest of brevity.

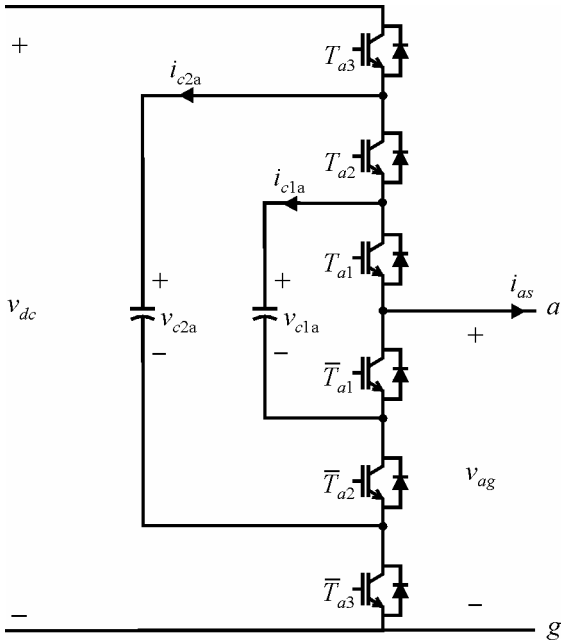


Figure 1. The three-cell FCMI inverter topology (a phase).

From Table II, it can be seen that there is considerable redundancy for the four-level case; having three possibilities for both intermediate levels E and $2E$. Although the redundant states have the same output voltages, they have different effects in terms of the capacitor currents. Therefore, a straightforward choice can be made which will improve the capacitor balance situation when the E or $2E$ level is required. For the five-level case, there is redundancy for all intermediate levels. However, it turns out that there is not enough redundancy to regulate the capacitor voltages. This problem will be solved by considering joint redundancy among all phases in a later section. As the number of voltage levels increases, the amount of redundancy goes down. For the eight-level case, each switching state has a unique voltage level and so there is no per-phase redundancy available.

TABLE II. THREE-CELL FCMI OUTPUT VOLTAGES WITH DIFFERENT RATIOS

T_{a1}	T_{a2}	T_{a3}	E : $2E$: $3E$	E : $2E$: $4E$	E : $4E$: $5E$	E : $3E$: $6E$	E : $3E$: $7E$
0	0	0	0	0	0	0	0
0	0	1	E	$2E$	E	$3E$	$4E$
0	1	0	E	E	$3E$	$2E$	$2E$
0	1	1	$2E$	$3E$	$4E$	$5E$	$6E$
1	0	0	E	E	E	E	E
1	0	1	$2E$	$3E$	$2E$	$4E$	$5E$
1	1	0	$2E$	$2E$	$4E$	$3E$	$3E$
1	1	1	$3E$	$4E$	$5E$	$6E$	$7E$
			four-level	five-level	six-level	seven-level	eight-level

III. MULTILEVEL VOLTAGE-SOURCE MODULATION

Voltage-source modulation can be accomplished in a multilevel inverter system using the sine-triangle method [11]. The first step is to define duty cycles for each phase as [17]

$$d_a = \frac{1}{2} \left[1 + m \cos(\theta_c) - \frac{m}{6} \cos(3\theta_c) \right], \quad (6)$$

$$d_b = \frac{1}{2} \left[1 + m \cos\left(\theta_c - \frac{2\pi}{3}\right) - \frac{m}{6} \cos(3\theta_c) \right], \quad (7)$$

$$d_c = \frac{1}{2} \left[1 + m \cos\left(\theta_c + \frac{2\pi}{3}\right) - \frac{m}{6} \cos(3\theta_c) \right], \quad (8)$$

where θ_c is the electrical angle which can be related to commanded frequency f^* by

$$\theta_c = 2\pi f^* t, \quad (9)$$

and m represents the modulation index which has a range from 0 to 1.15 [17]. The three duty cycles are compared to a set of triangle waveforms to produce commanded switching states for each phase. Figure 2 demonstrates the generation of switching state for the a -phase. In a digital signal processor (DSP) implementation, there is an alternate method of

producing the switching states which does not involve triangle waveforms [17].

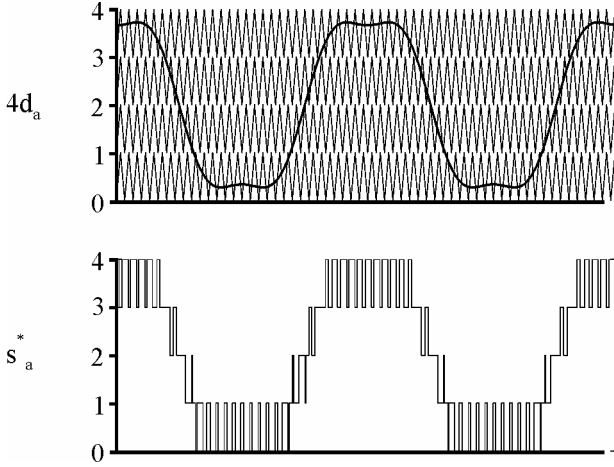


Figure 2. Five-level sine-triangle modulation.

IV. CAPACITOR VOLTAGE BALANCING METHOD

In order to obtain reasonable distinct multi-level output voltage results, the voltages on all six capacitors (two per phase) must be maintained at constant levels. However, the currents have different effects on the charging and discharging of the capacitors and will tend to unbalance the capacitor voltages. In this case, the redundant switching states become the key component for balancing the capacitor voltages.

Since there are several conduction paths within each phase which can produce the same voltage levels while having different capacitor charging characteristics, per-phase redundancy can be used to choose the path with the best balancing performance. However, for the same FCMI topology, as the number of achieved voltage levels increases, the number of available per-phase redundant states decreases. In this case, incrementing or decrementing the switching states of all three phases can also be used to balance capacitor voltages since this results in changes in the zero-sequence line-to-ground voltage, which does not affect the load phase voltages according to (4-5). The concept behind this joint-phase redundant state selection (RSS) method is that the line-to-ground voltages (v_{ag}, v_{bg}, v_{cg}) of all phases may be changed simultaneously without affecting the load voltages since the terms that are common in all phases will cancel when looking at the line-to-neutral voltages (v_{as}, v_{bs}, v_{cs}) or line-to-line voltages (v_{ab}, v_{bc}, v_{ca}). For example, the state involving ($v_{ag} = 0, v_{bg} = E, v_{cg} = E$) could be changed to ($v_{ag} = E, v_{bg} = 2E, v_{cg} = 2E$) or ($v_{ag} = 2E, v_{bg} = 3E, v_{cg} = 3E$) or ($v_{ag} = 3E, v_{bg} = 4E, v_{cg} = 4E$). Even though the load voltages do not change, the selection of the appropriate joint state can improve the capacitor balancing situation. In this paper, two joint-phase redundant state selection algorithms are introduced.

A. On-line Joint-Phase RSS

A direct balancing algorithm can be used if phase current measurement is available. In general, this algorithm for JRSS

works as follows. With the desired levels for each phase, all joint redundant states are considered (as well as per-phase sub-choices). Assuming that phase currents do not change during one DSP switching period (t_s), which is always valid when the switching frequency is high, the predicated capacitor voltage change for each state can be calculated as

$$\Delta v_{c_{yx}} = \frac{i_{c_{yx}} \cdot t_s}{C_y} \quad (10)$$

where x is the phase (a, b , or c), y is the capacitor (1 or 2). The capacitor currents $i_{x_{cy}}$ are determined from phase current sensors and the inverter switching path. Predicted capacitor voltages are determined for each state as

$$\tilde{v}_{c_{yx}} = v_{c_{yx}} + \Delta v_{c_{yx}} \quad (11)$$

The square error for each potential state is evaluated by comparison to ideal voltages as

$$\mathcal{E} = \sqrt{\sum_{x=a}^c \sum_{y=1}^2 (v_{c_{yx}}^* - \tilde{v}_{c_{yx}})^2} \quad (12)$$

and the state with the least error is chosen. This algorithm minimizes the error between capacitor voltages and their ideal values, and thus gives the best possible choice to improve the overall balancing of voltages of the six capacitors.

B. Look-up Table Joint-Phase RSS

The look-up table method requires that the direction of the three-phase load currents be known. Then the direction of capacitor currents can be determined considering transistor switching state from (2) and (3). The multilevel modulator determines desired levels for each phase then all joint redundant states and per-phase sub-choices are considered. Capacitor current direction flags are used to determine whether a choice is improving or worsening the capacitor balancing situation. Since there are two capacitors in one phase, for each switching state, its overall effect on six capacitors must be considered. If the capacitor current direction is positive (out of capacitor) and the capacitor is overcharged, this redundant state will help regulate the capacitor voltage. Similarly, if the current direction is negative and the capacitor is undercharged, the redundant state will also help regulate the capacitor voltage. A balancing performance index is chosen to describe the capacitor charging and discharging characteristics of each state. The switching state with the highest performance index is selected. The performance indices for each switching state in all possible situations are pre-calculated and compared so that the best state can be obtained directly from a table based on load current direction flags and capacitor voltage flags. All these flags form the address (index) of the table. Let F_{ix} represent the capacitor current direction flag, which equals to 1 for positive current and 0 for negative current. Let F_{vx} represent the capacitor voltage flag, which is defined as

$$F_{vx} = \begin{cases} 1 & v_{c_{yx}} \geq v_{c_{yx}}^* \\ 0 & v_{c_{yx}} < v_{c_{yx}}^* \end{cases} \quad (13)$$

Still two more flags are necessary. One is $F\Delta_{cx}$, which is defined as

$$F\Delta_{cx} = \begin{cases} 0 & \frac{\text{abs}(v_{c1x} - v_{c1x}^*)}{v_{c1x}^*} \geq \frac{\text{abs}(v_{c2x} - v_{c2x}^*)}{v_{c2x}^*} \\ 1 & \frac{\text{abs}(v_{c1x} - v_{c1x}^*)}{v_{c1x}^*} < \frac{\text{abs}(v_{c2x} - v_{c2x}^*)}{v_{c2x}^*} \end{cases} \quad (14)$$

The other is $Ind\Delta_c$, representing which capacitor in six capacitors should be balanced first.

C. Operating Modes of the Distended FCMI

The proposed algorithms were evaluated through detailed simulation. The JRSS method works better for lower modulation indices since that leads to more available joint states. As a worst-case analysis, consider the results of Figure 3. Therein, the modulation index is set to a maximum and the maximum power factor (without loosing capacitor voltage balance) is shown for the various numbers of levels for the three-cell FCMI. From Figure 3, it can be seen that the four-level case will maintain balance under all circumstances. The five-level will work for power factors up to 0.88 lagging. This makes the five-level suitable for motor drives where the power factor is typically below 0.8 lagging at full modulation index. For six- seven- and eight- level operation, capacitor voltage balance is only possible for lower power factors. In this case, this performance is only achievable for reactive power applications such as static var compensation.

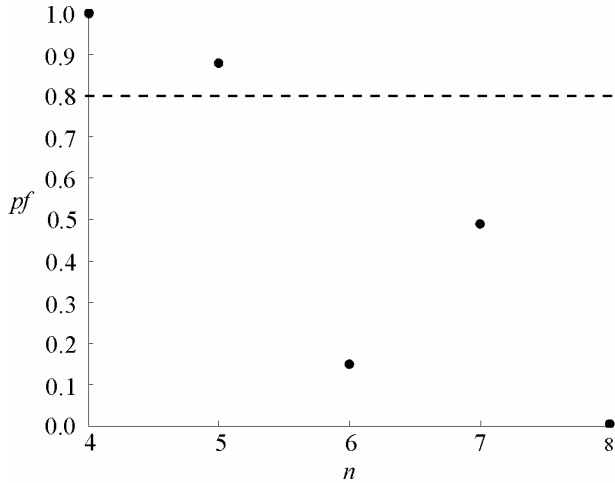


Figure 3. Maximum power factor versus number of levels.

V. COMPUTER SIMULATION RESULTS

A. Steady-State Study

A computer simulation has been created to verify the proposed method. Figure 4 shows the inverter waveforms for five-level operation at near maximum modulation index ($m = 1.14$) with a power factor of 0.81 lagging. In this simulation, a three-phase RL load is connected to inverter with $Z = 4.84 \Omega$. The input is set to $v_{dc} = 200$ V. The capacitor voltage balance can be seen in that the line-to-ground voltage has five distinct levels. The effect of JRSS is seen in the bus clamping to the highest and lowest levels. However since this is done in all phases, the line-to-neutral and line-to-line voltages are not affected. Figure 5 shows the eight-level operation at modulation index $m = 0.9$ and 0.25 lagging. Again, capacitor balance is evident considering the even levels of v_{ag} and v_{ab} .

B. Dynamic Studies

Motor drive operation is shown in Figure 6. Therein, the three-cell FCMI inverter drives an induction motor with vector control and an outer speed loop. The speed command is ramped up to 188 rad/s. A step change in load from 0 to 20 N·m is applied at 4.5s then the commanded speed is lowered to zero with the load on the motor. In this case, the input source is set to $V_{dc} = 660$ V. The torque, speed, and capacitor voltages shown in Figure 6 indicate good balance throughout this dynamic study as the modulation index and power factor change over a wide range.

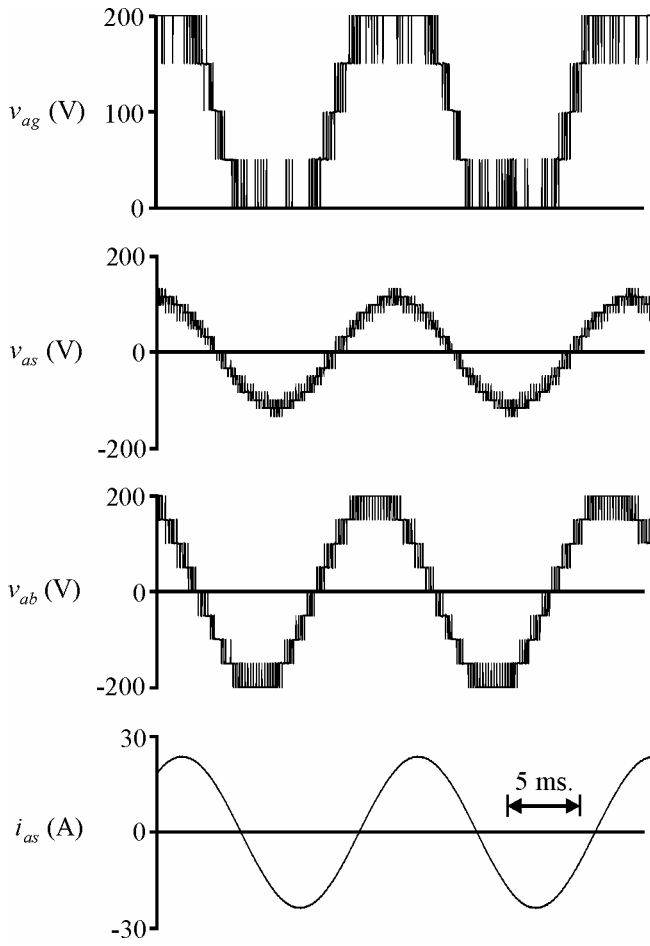


Figure 4. Five-level steady-state operation.

VI. LABORATORY VALIDATION

In order to validate the proposed concept, a three-cell 5-level FCMI inverter was constructed in the laboratory. Figure 7 shows a block diagram of how the balancing algorithm was implemented. The modulation is programmed in a DSP which outputs desired switching states, as described above, which are labeled s_a^* , s_b^* , and s_c^* . Analog-to-digital conversion is performed on the phase current and capacitor voltages in order to determine the current direction and capacitor voltage flag. This information along with the desired switching state forms the address of the desired state in the redundant state selection table. Redundant states were calculated off-line and programmed into a complex programmable logic device (CPLD).

The ratio of the capacitor and DC source voltages was set to 1:2:4. A 3.7 kW induction motor was used as a load. The dc voltage v_{dc} was supplied from an isolated rectified three-phase source and had a voltage of 200V. The capacitance values of the capacitors were $C_1 = C_2 = 3300$ uF. The modulation parameters for this test were $m = 1.14$ and the commanded fundamental frequency f^* was 60Hz. Figure 8 shows the resulting capacitor voltage v_{c1a} , v_{c2a} , line-to-neutral voltage

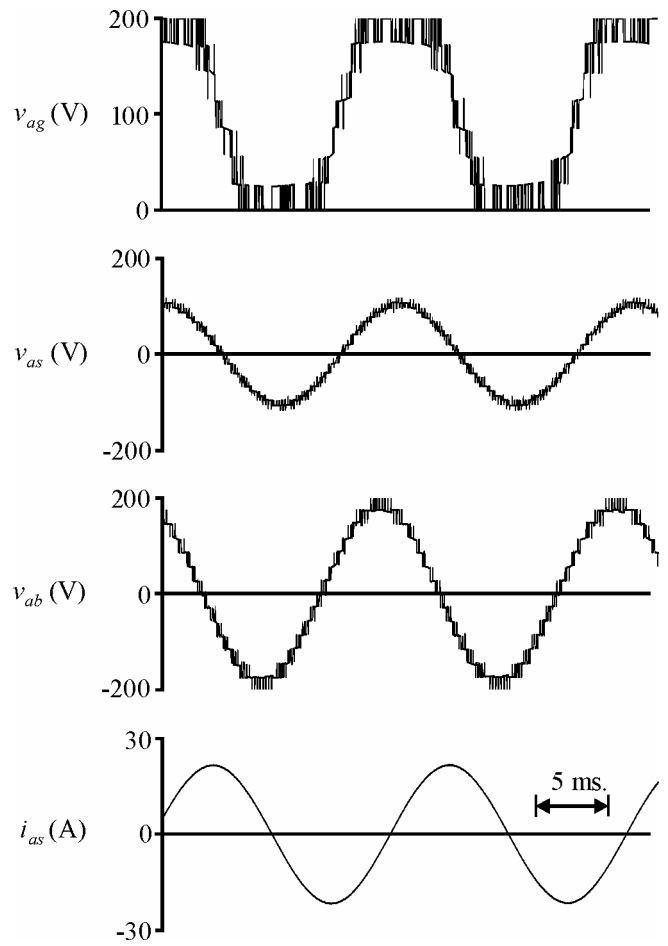


Figure 5. Eight-level steady-state operation.

v_{ag} , line-to-line voltage v_{ab} and load current i_{as} . As can be seen, the voltages and currents exhibit typical 5-level inverter performance. Since the ratio of voltages was set to 1:2:4, the laboratory results show the capacitor voltages can be regulated at $v_{c1a} = 50$ V and $v_{c2a} = 100$ V. The low frequency harmonics seen in the current waveform are due to induction motor saturation.

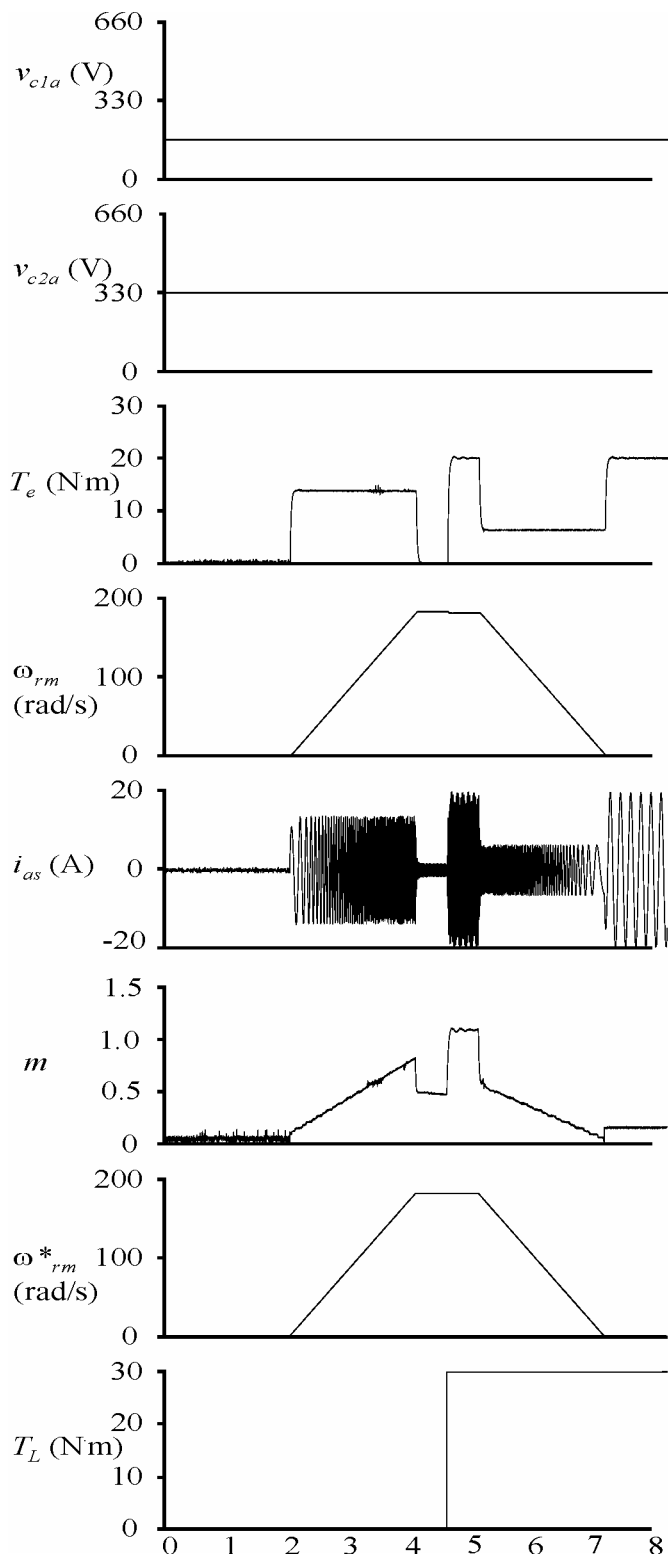


Figure 6. Five-level dynamic motor drive operation.

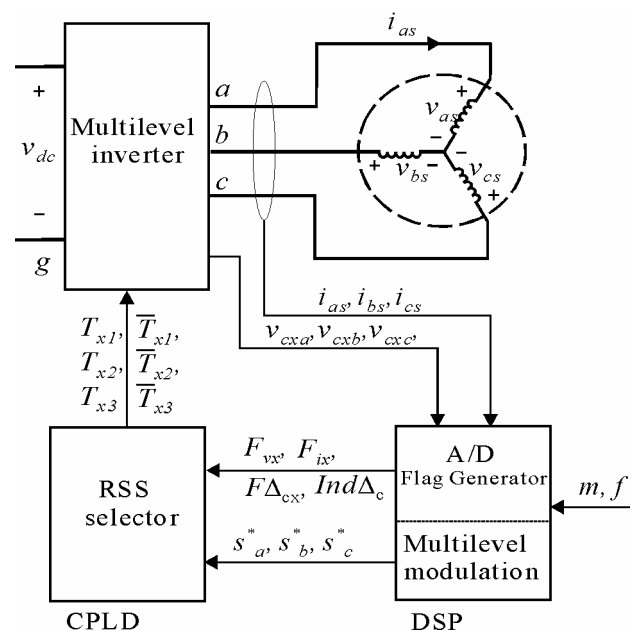


Figure 7. Five-level inverter implementation.

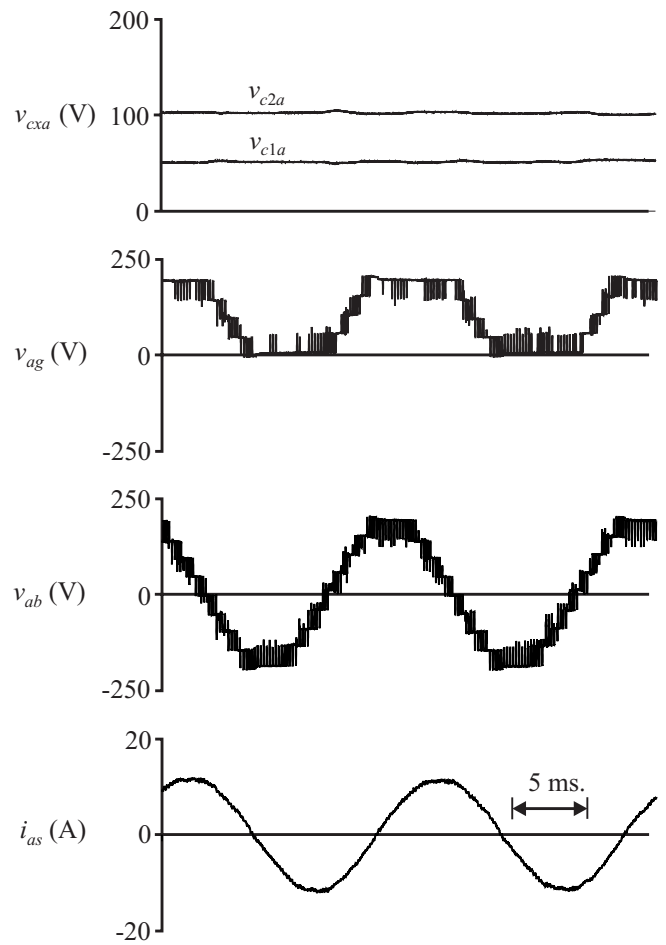


Figure 8. Five-level inverter laboratory test results.

VII. CONCLUSION

This paper has studied extended operation of a three-cell flying capacitor multi-level inverter. Redundant switching states, vital to capacitor voltage balancing, are sacrificed to achieve a higher number of output voltage levels. Two joint-phase redundant state selection algorithms were proposed to keep the capacitor voltages constant. Simulation results demonstrate the effectiveness of each algorithm. One algorithm was validated with laboratory experiments on a motor drive system. In that study, a three-cell flying capacitor inverter which typically operates in the four-level mode was extended to five-level operation. It was also demonstrated through simulation that the three-cell inverter can achieve eight-level operation for applications involving reactive power compensation.

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